Features

- Frequency：8~12 GHz
- Saturation Pout：43dBm @40%PAE
- Operation Voltage：+28V@1.9A
- Input/Output Impedance：50 Ohm
- Dimension：3mm x 2mm x 0.08mm
- Power Gain：20dB

Electrical Specification (T_A=+25°C，50Ω system，V_{dd}=28V，V_{gg}=-2.0V)

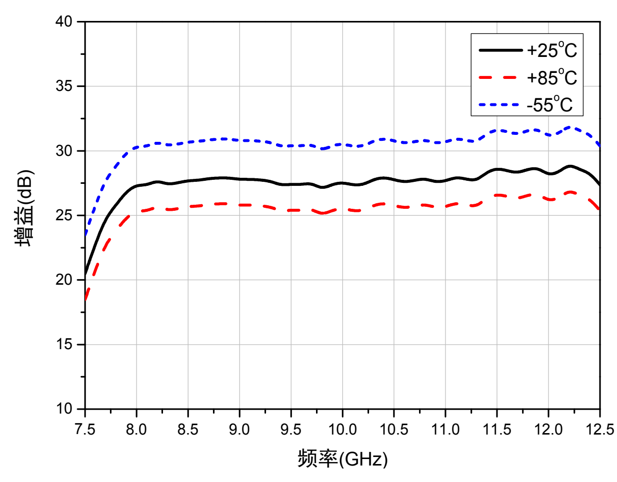
Parameter	Min.	Typ.	Max.	Unit
Frequency	8-12			GHz
Power Gain		20		dB
Saturation Pout		43		dBm
P.A.E		40		%
Operation Current		1.8		A

Limited Rating Values

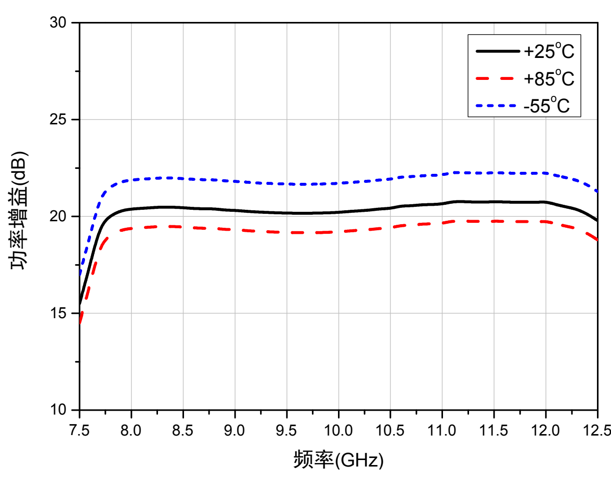
Vdd	+33V
RFInput Power	+28dBm
Junction Temperature	+200°C
Storage Temperature	-65~+150°C
Operating Temperature	-55~+125°C

Typical Testing Curves

Small Signal Gain VS Temperature



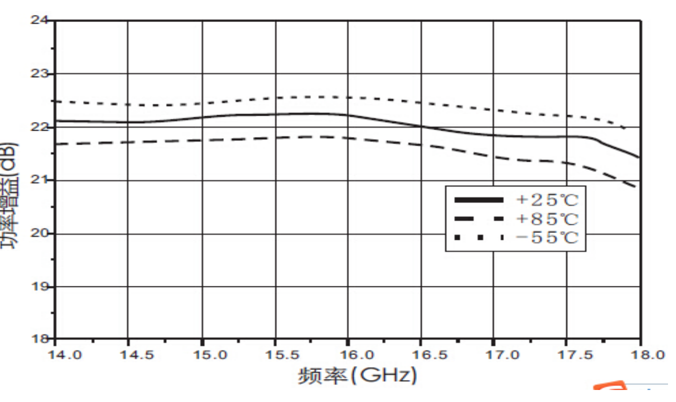
Power Gain VS. Frequency



Features：

- Frequency：14～18 GHz
- Saturation Pout：42dBm@36 P.A.E
- Power Gain：20 dB
- Operation Voltage：28 V/1.7A
- Input/Output Impedance 50Ω
- Dimension: 3.0*2.0*0.08 mm

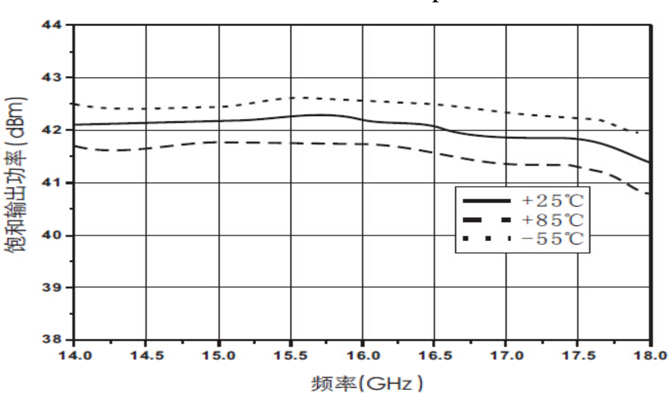
Power Gain VS Frequency



Electrical Specification（TA=+25℃, Vdd=28V, Vgg=-1.8V）

Parameter	Min.	Typ.	Max.	Unit
Frequency		14-18		GHz
Power Gain	19	20		dB
Saturation Pout	41	42		dBm
P.A.E		36		%
Operation Current		1.7		A

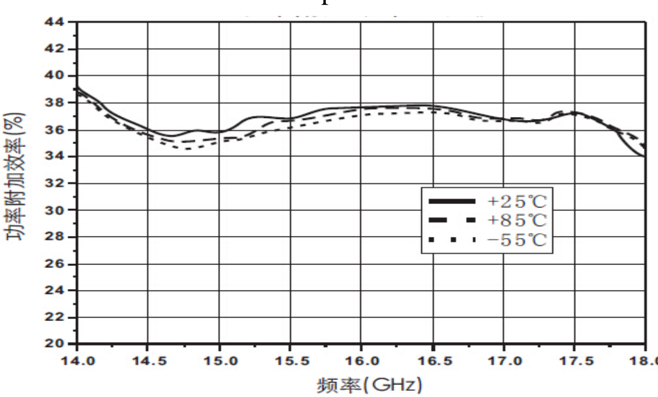
Saturation Pout VS Temperature



Limited Rating Values

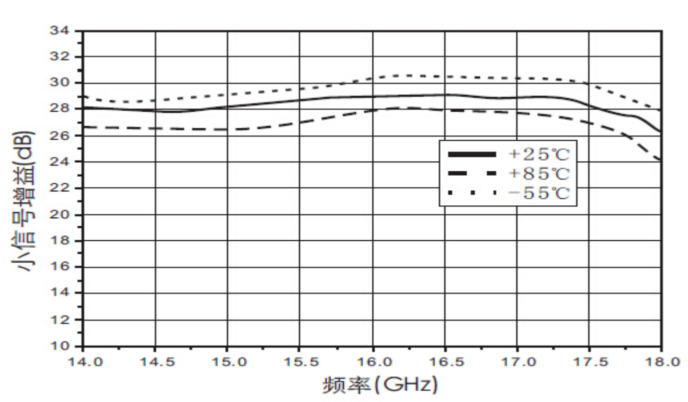
Vdd	+33 V
RF Input Power	+30 dBm
Storage Temperature	-65℃～+150℃
Operating Temperature	-55℃~+125℃
Static Protection(HBM)	Class 1A
Junction Temperature	175℃

P.A.E VS Temperature

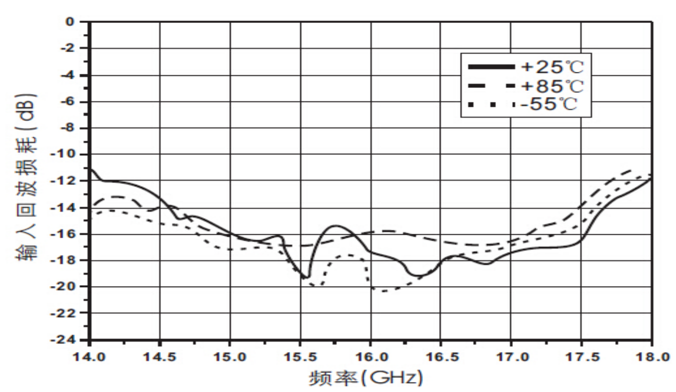


Typical Testing Curves

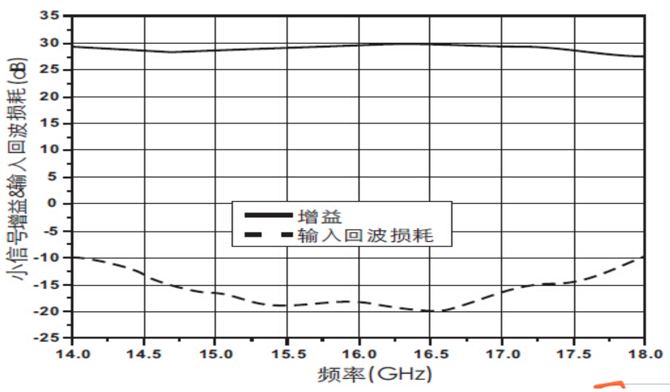
Small Signal Gain VS Temperature



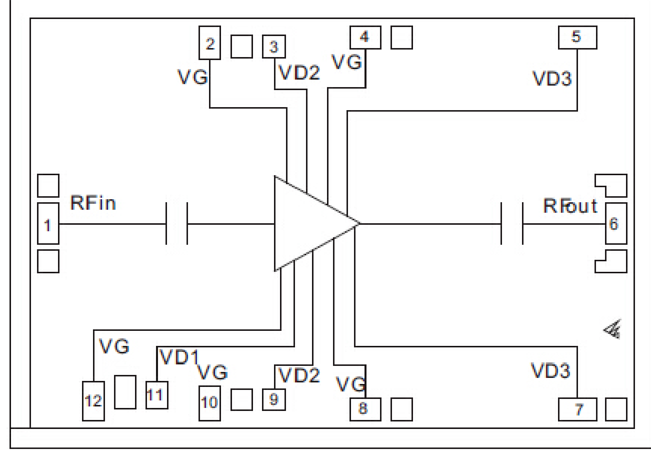
Input Return Loss VS Temperature



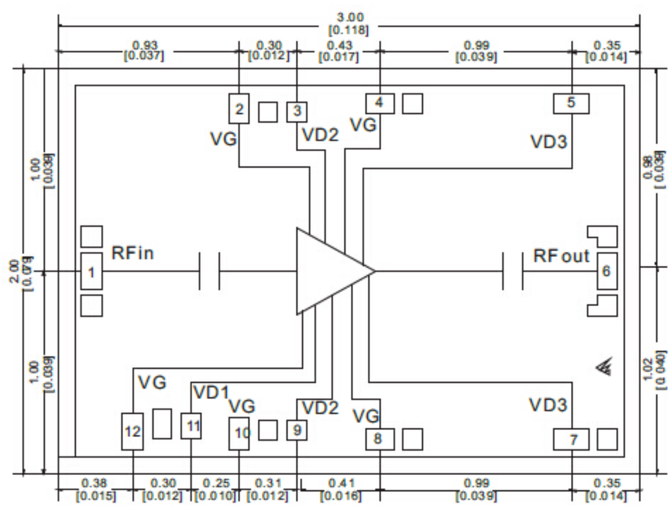
Small Signal Gain VS Return Loss



Block Diagram



Dimension and Outline



Remarks

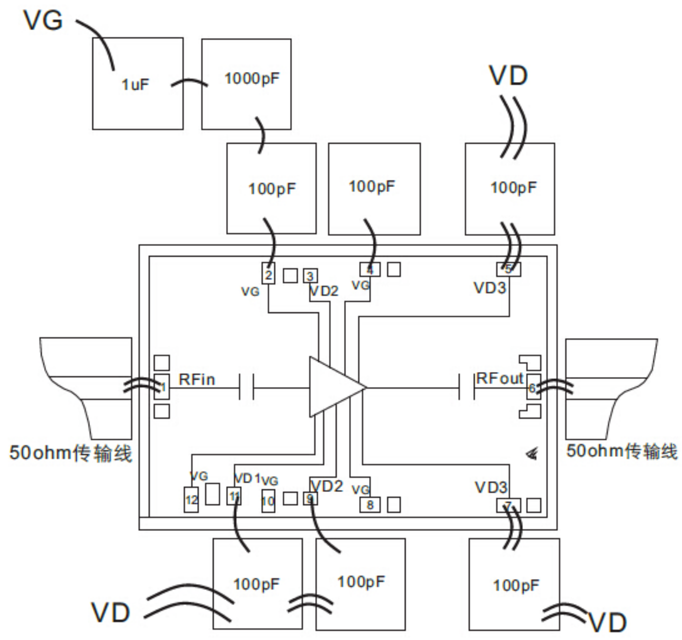
1. Unit mm
2. Backside of MMIC gold plated and grounded
3. Bonding pad shall be gold plated
4. No bonding on the via hole
5. Dimension tolerance: ±0.05 mm
6. Pad dimension:

1,5,6,7: 0.18*0.10 mm
2,4,8,10:0.145*0.1mm
3,9:0.1*0.1mm
11:0.125*0.1mm

Bonding Pin Definition

Number	Function	Description
1	RF Input	RF input, 50Ω Impedance, no blocking capacitor is needed
3,5,7,9,11	Vd	External 100pF needed
2,4,8,10,12	Vg	100pF,1000pF, 1uF needed
6	RF output	RF output, 50 Ω Impedance, no blocking capacitor is needed
Back	GND	

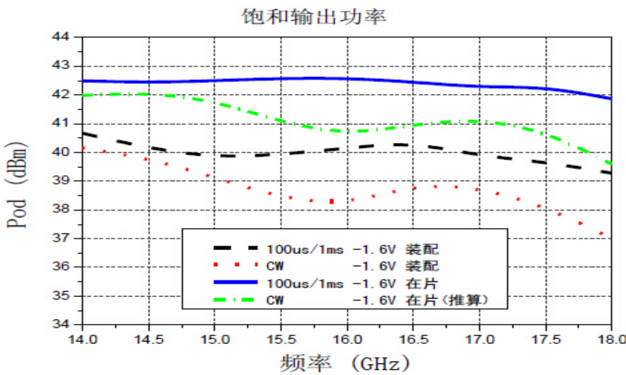
Assembly Chart



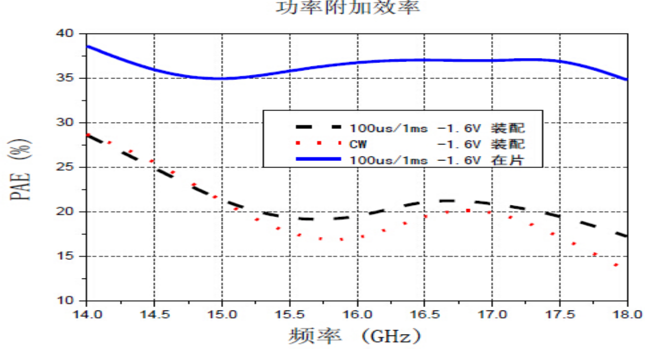
Additional CW Testing Results

Testing Condition:
Vdd=+28V, Vgg=-1.6V;
Input Power Pin=20dBm
Pulse condition, Pulse width 100 μ s, duration 1 ms, Duty cycle 10%.

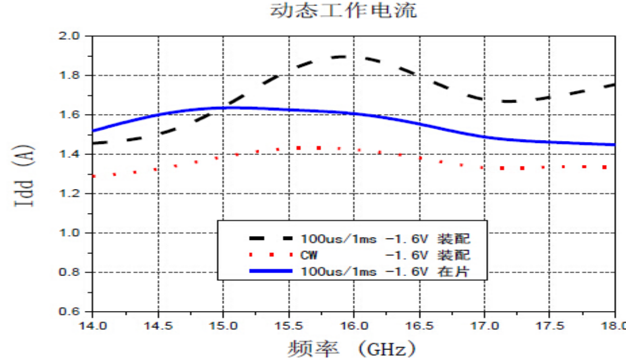
Saturation Pout



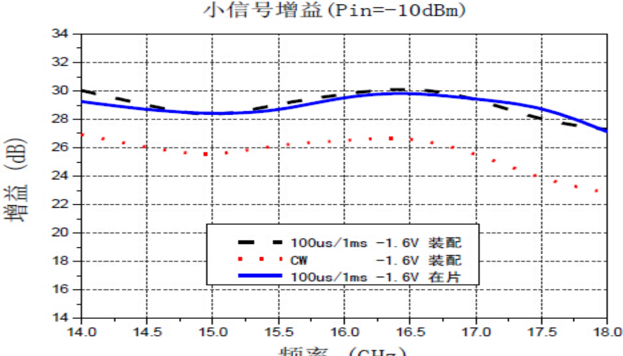
P.A.E



Dynamic Current



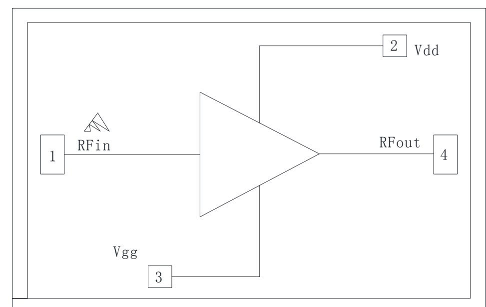
Small Signal (Pin=-10dBm)



Characteristics

- Frequency：8.0~12.0 GHz
- Psat Output Power：26 dBm
- Power Gain：16 dB
- DC Power Supply：+28V@130 mA
- Input and Output Impedance：50 Ohm
- Dimension：1.8 x 1.4 x 0.1mm

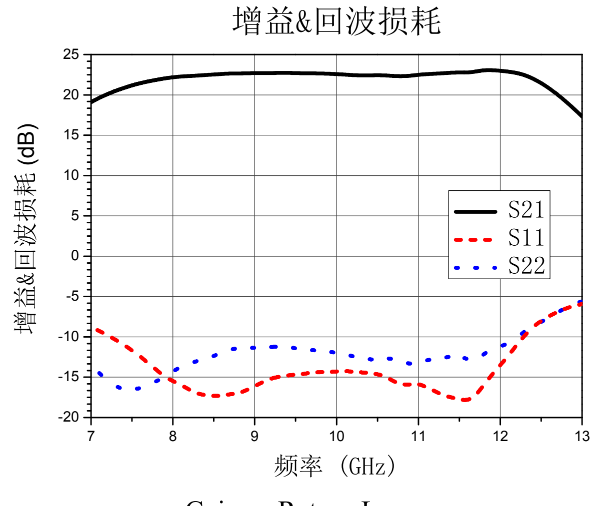
Block Diagram



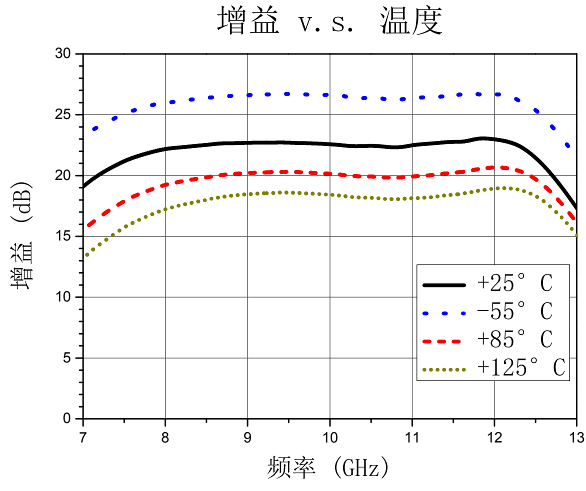
Electrical Specification (TA =+25°C，50Ω system，Vdd=28V，Vgg=-2V)

Parameter	Min	Typical	Max	Unit
Frequency	8.0-12.0			GHz
Gain		22		dB
Saturation Power (Psat)		26		dBm
Input Return Loss		14		dB
Output Return Loss		11		dB
Operation		130		mA

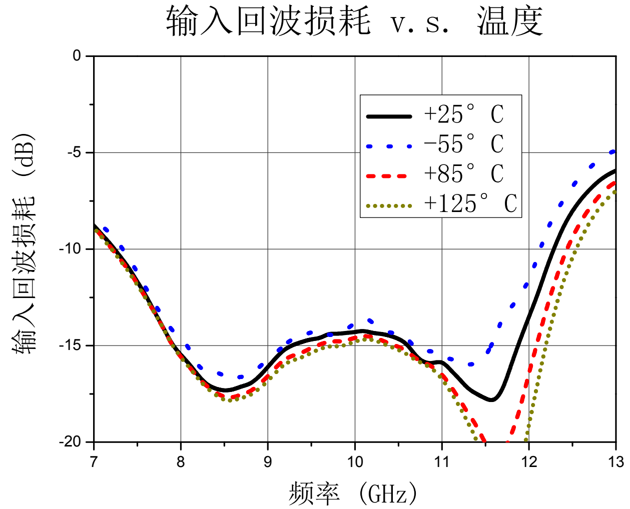
Testing Curves



Gain vs Return Loss

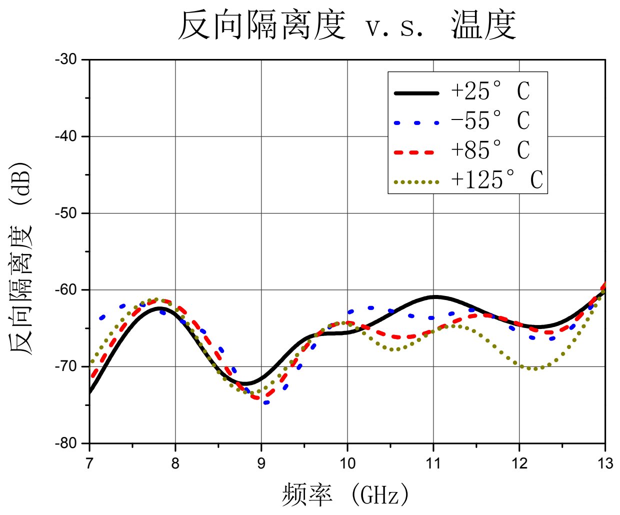


Gain vs Temperature

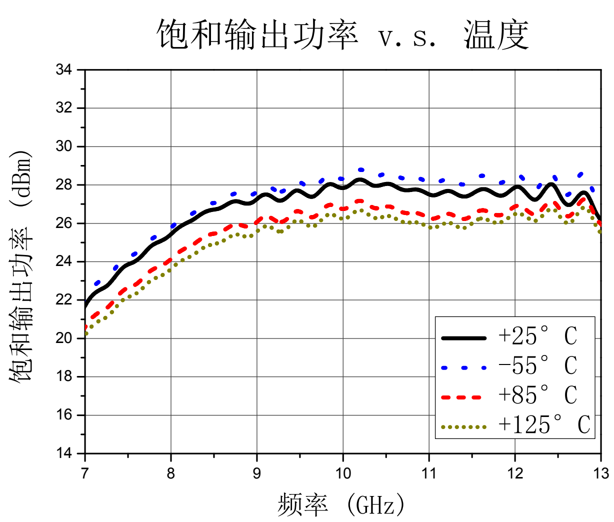


Input Return Loss vs Temperature

Output Return Loss vs. Temperature



Reverse Isolation vs. Temperature

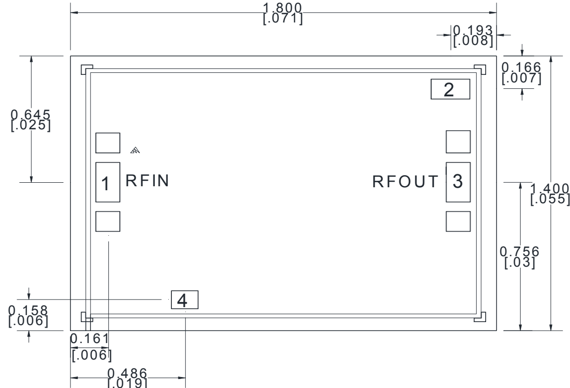


Psat Output vs. Temperature

Limited Rating Value

Power supply voltage	+33 V
RF Input Power	+20 dBm
Max Junction Temperature	200°C
Storage Temperature	-65~+175°C
Operation Temperature	-55~+85°C

Dimension



Notice：

1.unit：mm[inches]

2. Backside golden plated

3. Backside back grounded

4. Bonding pad golden plated, pad dimension：0.1mmx0.2mm

5. no bonding on via hole

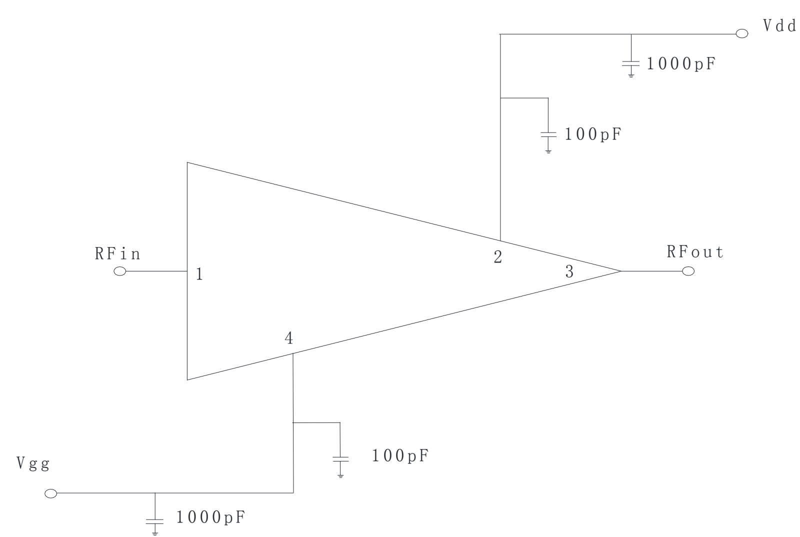
6. Tolerance：±0.05mm

Pad Definition

NO.	Functions	Description	Circuit
1	RFIN	RF signal input terminal, an external 50 ohm system, No need for blocking capacitors	RFin
2	Vdd	Amplifier drain bias voltage, it needs an external 100Pf 、1000pF bypass capacitor	Vdd
3	RFOUT	RF signal output terminal, an external 50 ohm system, No need for blocking capacitors	RFout

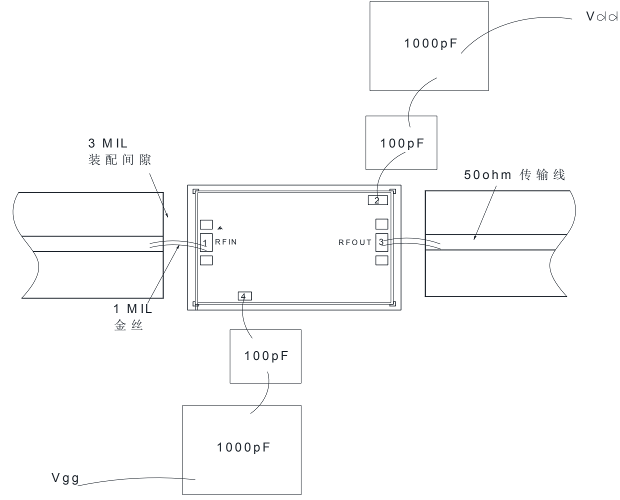
4	Vgg	Amplifier gate bias voltage, it needs an external 100Pf 、 1000pF bypass capacitor	Vgg
Backside	GND	Ground	GND

Typical Circuit Structure



Application

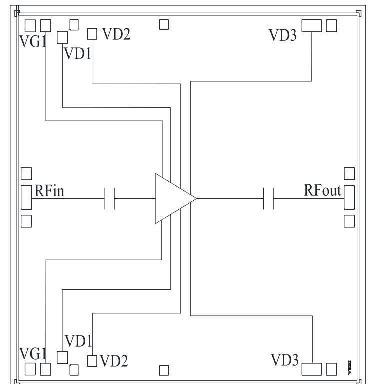
Assembly Drawing



Features

Frequency ： 8~12 GHz
Psat ： 46dBm @38%PAE
Power Gain： 22dB
Operating Voltage： +28V@3.9A
Input / Output Impedance： 50 Ohm
Dimension ： 4.15mm x 5.5mm x 0.08mm

Functional Diagram

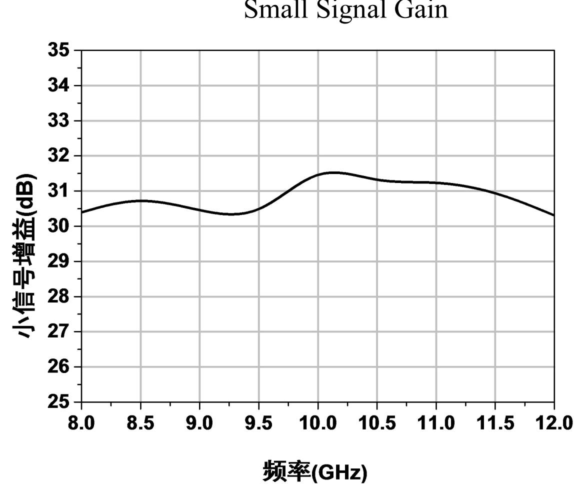


Electrical Specification(T_A=+25°C，50Ω system，V_{dd}=28V，V_{gg}=-1.8V（Typ），I_{qd}=2.0A)

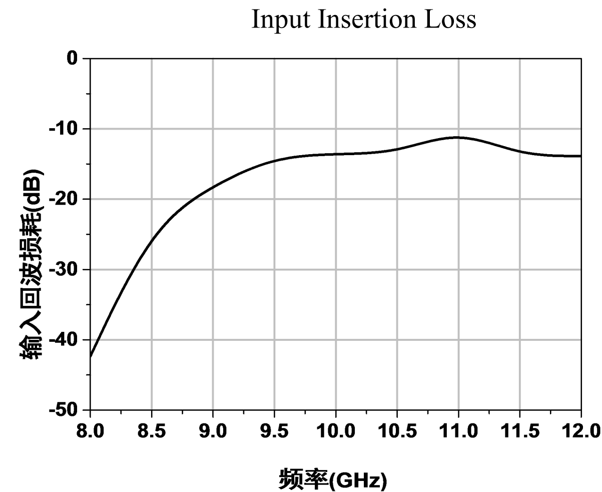
Parameter	Min	Typ	Max	Unit
Frequency	8-12			GHz
Power Gain		22		dB
Psat		46		dBm
PAE	38	-		%
Operating Current		3.8		A

Testing Curve

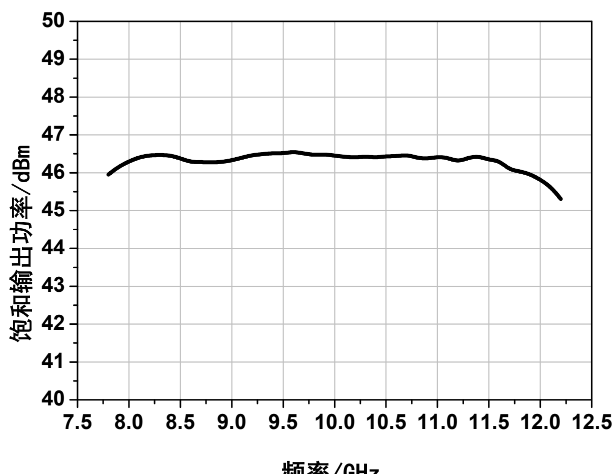
Small Signal Gain



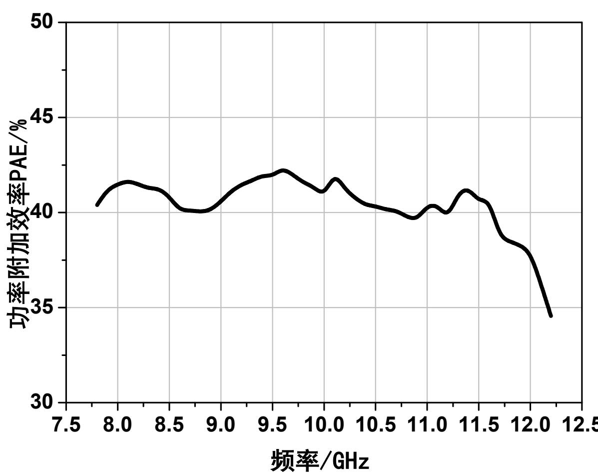
Input Insertion Loss



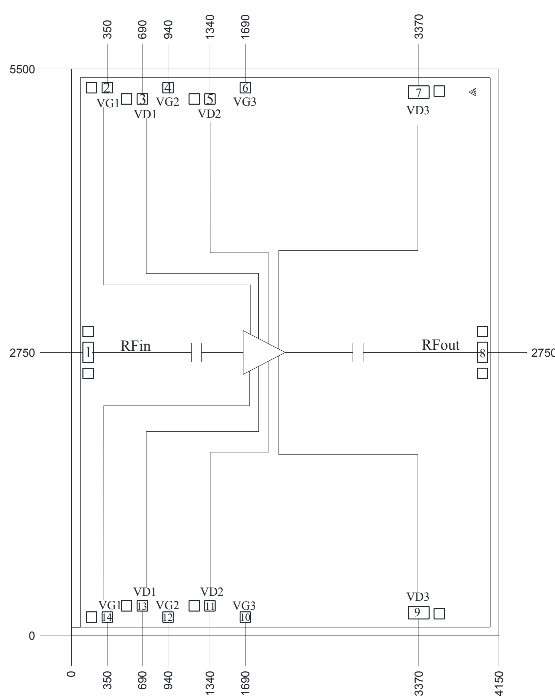
Psat vs. Frequency (Pin:24dBm)



PAE vs. Frequency (Pin:24dBm)



Dimension



Instruction ：

1.unit ： mm[inch]　　　　　2. gold-plated on the back of the mmic

3.the back of the mmic ground

4.bonding pad is gold plated

pad dimension： 1、7、8、9： 0.20mmx0.10mm；

2、3、4、5、6、10、

11、12、13、14：0.10mmx0.10mm

5.can not be bonded on the through-hole

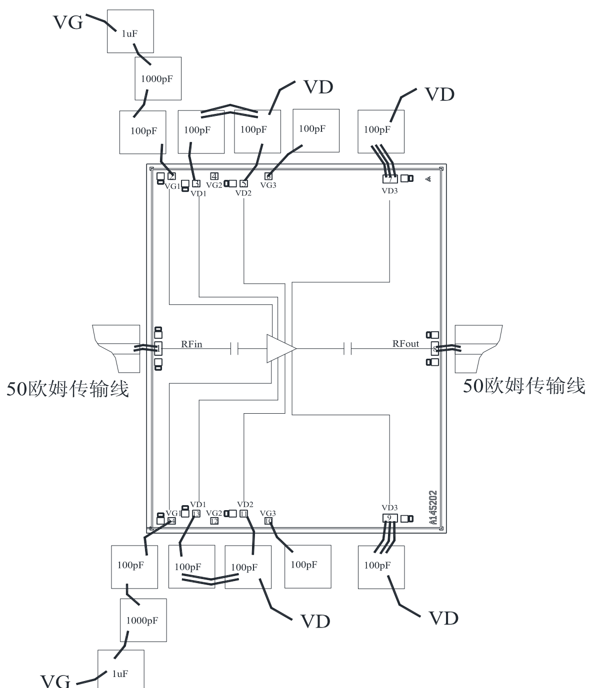
6.dimension tolerance：±0.05mm

Bonding pad Definition

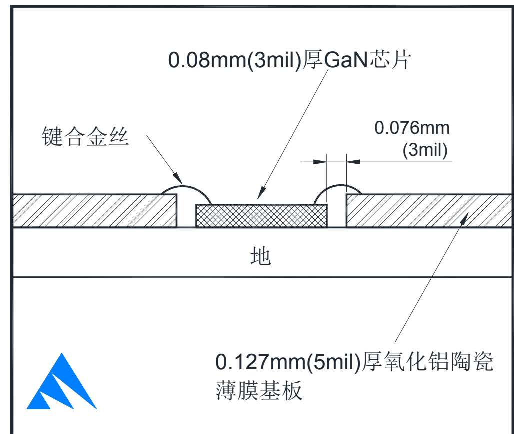
Pad Number	Function symbol	Function Description	Equivalent Circuit
1	RFin	RF signal input terminal, an external 50 ohm system, Without blocking capacitors	RFin
3、5、7、9、11、13	V_D	Amplifier drain bias voltage, it need an external 100pF bypass capacitor	Vdd
2、4、6、10、12、14	V_G	Amplifier gate bias voltage, it need an external 100Pf 、1000pF、1uF bypass capacitor	Vgg
8	RFout	RF signal output terminal, an external 50 ohm system, Without blocking capacitors	RFout
	GND	Ground	GND

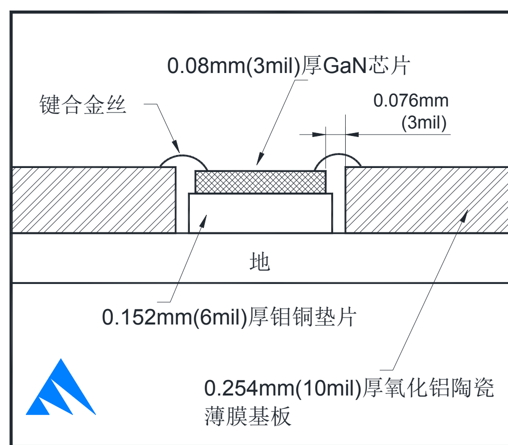
Application

1. Assembly Diagram (Filter capacitor should be close to the chip to minimize the impact of the bond wire length)



2. Assembly Instruction





Note : Ceramic substrate should be as close as possible to shorten the bonding wire chip size. Typical assembly clearance is 0.076~0.152 mm (3 ~ 6 mils)

Features

- Frequency：13.5GHz～15.5GHz
- Power Gain：20dB
- Psat：45dBm
- P.A.E.：30％
- +28V @ 2.5A（Quiescent）
- Chip Size：4.0mm×3.7mm×0.1mm

Electrical Specification（TA=+25℃,Vd=+28V，Vg=-2.5V）

Parameter	Min.	Typ.	Max.	Unit
Frequency	13.5-15.5			GHz
Power Gain	19	20		dB
Psat	44.8	45.2		dBm
P.A.E.	30	33		％
VSWRin			2.5	-
Dynamic Operating Current	3.5			A

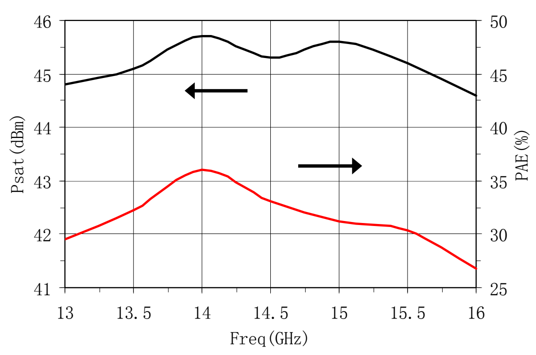
Note：1）All chips have been on-chip 100% DC tested.
2) Test Condition：Vd=+28V，Vg=-2.5V, pulse width 100μs，duty cycle 10%，P_{in}=25dBm.

Limited Rating Values

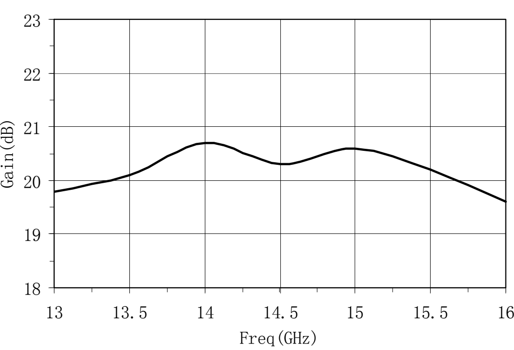
Max. Input Vd	+30V
Max. Input Power	+30dBm
Storage Temperature	-65℃～+150℃
Operating Temperature	-55℃～+85℃

Typical Testing Curves

Output Psat/Efficiency VS Frequency

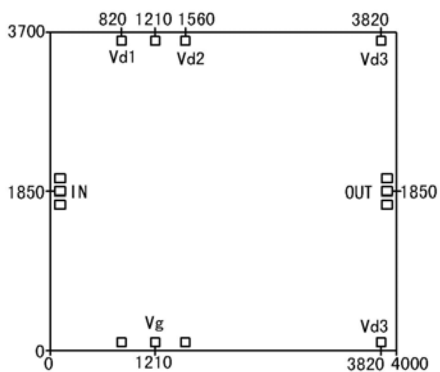


Power Gain VS Frequency



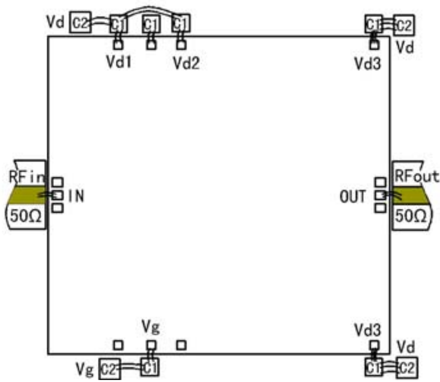
Dimensions and Outline

NC11602C-1315P30 outline



Note：The unit is um. Dimension of input/output pad: 100×120μm². Dimension of bias pad: 100×100μm².

Assembly Diagram



Note： External capacitor c=100pF,c2=0.01μF. A 0.01μF capacitor should be added to gate bias. Diameter of gold wires: 25μm.

Attention

1) 2 bonding wires should be used for input/output. The length should be shorter than 350μm.
2) Bonding with 80/20 Au/Sn. The temperature should be lower than 300℃ and time should be less than 30 seconds.
3) Blocking capacitors in Input/Output are already integrated.
4) Antistatic protection should be taken.

Features:

- Frequency: 8.5～10.5GHz
- Power Gain: 20dB
- Psat: 44.8dBm
- P.A.E.: 38%
- +28V @ 2.5A (static)

Electrical Specification (TA=+25 ℃ ,Vd=+28V , Vg=-3~-2V)

Parameter	Min.	Typ.	Max.	Unit
Frequency	8.5-10.5			GHz
Power Gain	20.8	21.4	-	dB
Output Psat	44.8	45.4	-	dBm
P.A.E.	36	38	-	%
VSWRin	2.0	-	-	—
Operating Current		3.3	3.8	A

Note: 1) All chips have been 100% DC tested

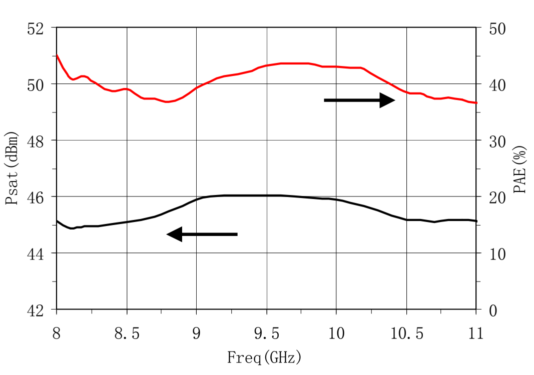
2) RF test condition: Vd=28V, Vg=-3~-2V, Pin=24dBm, D=40%, τ =6ms.

Limited Rating Values

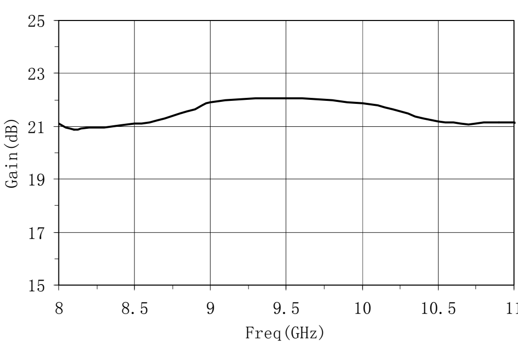
Max. Input VD	+30V
Max Input Power	+27dBm
Storage Temperature	-65℃～+150℃
Operating Temperature	-55℃～+125℃

Typical Testing Curves

Output Psat /Efficiency VS Frequency

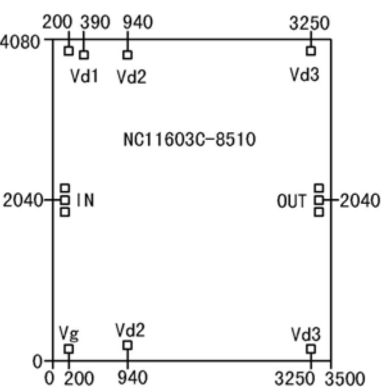


Power Gain VS Frequency



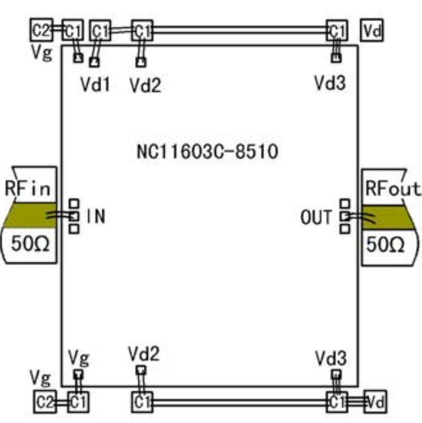
Dimensions and Outline

NC11603C-8510 outline



Note: All units in um.
Dimension of Input/Output Pad 100×100um^2.

Assembly Diagram



Note: External capacitor C1=100pF,C2=0.01uF; Diameter of bonding gold wires: 25um.

Features

- Frequency：8GHz-12GHz
- Power Gain：20dB
- Psat：42dBm
- P.A.E：38%
- +28V@0.7A(Quiescent)
- Dimension：2.0mm×3.0mm×0.1mm

Electrical Specification（TA=+25℃，Vd=+28V，Vg=-2V）

Parameter	Min	Typical	Max	Unit
Frequency	8-12			GHz
Saturation Pout		42		dBm
Power Gain		20		dB
Small Signal Gain Flatness		±2.5		dB
P.A.E	38			%
VSWRin		1.6	2.2	-
Operation Current	1.5			A

Note：1）all chips have been 100% DC and RF tested.

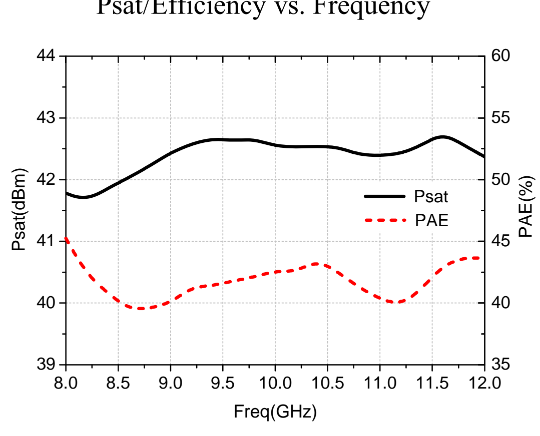
2）Test condition:Vd=+28V，Vg=-2V，P_{in}=22dBm，pulse width：100μS，duty cycle：10%

Limited Rating Values

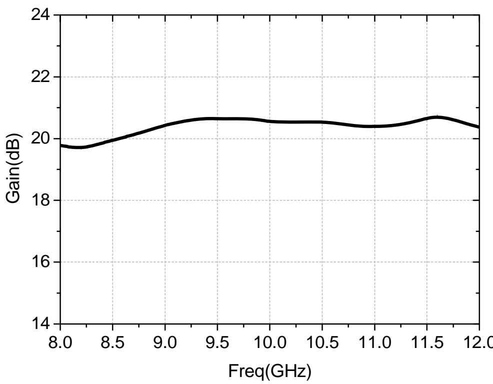
Max Vds	+32V
Min Vgs	-3V
Max Input Power	+25dBm
Operation Temperature	-55℃～+125℃
Storage Temperature	-65℃～+150℃

Typical Testing Curves

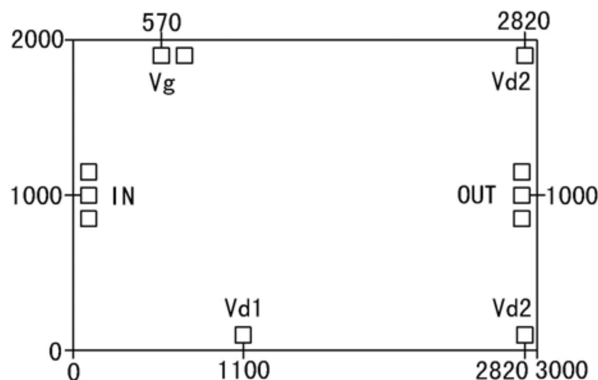
Psat/Efficiency vs. Frequency



Power Gain vs. Frequency

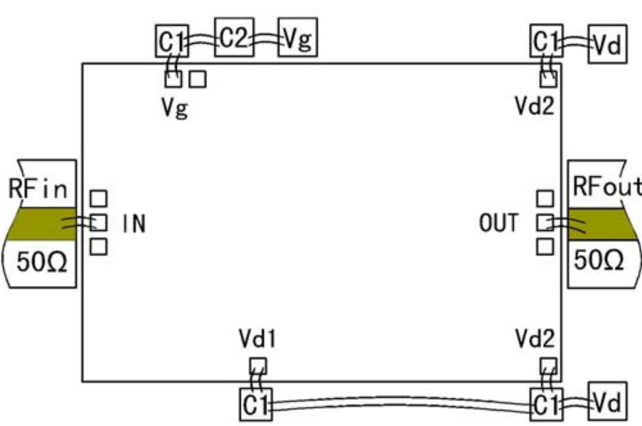


Dimension and Outline



Note：all units are(μm), dimension of input and output pad 100×100μm^2，
Dimension of Bonding pad Vd 100×100μm^2，tolerance of dimension ±50μm

Assembly Chart



Note：external capacitor of C1 value is 100pF，C2 is 1000pF

Attention：

1) Two Gold wires (diameter: 25μm) are suggested for bonding. The temperature of bonding platform shall not exceed 250℃. Length shall be less than 400 um.

2) Bonding with 80/20 Au/Sn. Temperature should be lower than 300℃ and time should be less than 30 seconds.

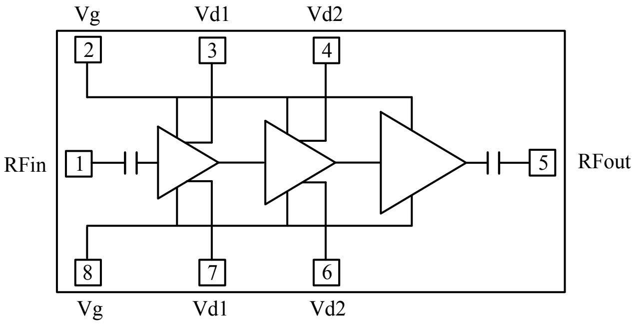
3) Blocking capacitors in Input/Output are already integrated.

4) When power on, put Gate Voltage first, then Drain Voltage. When power off, lower down Drain Voltage first, then Gate Voltage.

Features

- Frequency：8.0GHz～12.0GHz
- Power Gain：20dB
- Psat：42dBm
- P.A.E.：35%
- +28V@400mA(static)
- Chip Size：2.60mm×2.00mm×0.08mm

Functional Block Diagram



DC Electrical Specification（TA＝+25℃）

Parameter	Symbol	Min.	Typ.	Max.	Unit
Gate Voltage	Vg		-2.3	-5	V
Drain Voltage	Vd		28	32	V
Static Drain Current	Id		400		mA
Dynamic Drain Current	Idd		1.4	1.5	A
Dynamic Gate Current	Igg		0.1	0.2	mA

Microwave Electrical Specification（TA＝+25℃，Vd＝+28V）

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency	f	8～12			GHz
Psat	Psat	41.7	42		dBm
Power Gain	Gp	19.7	20		dB
Power Gain Flatness	△Gp			±0.4	dB
P.A.E.	PAE	35			%
Linear Gain	Gain		29	32	dB
Linear Gain Flatness	△Gain			±2	dB
VSWRin	VSWR(in)		1.6	2.2	-

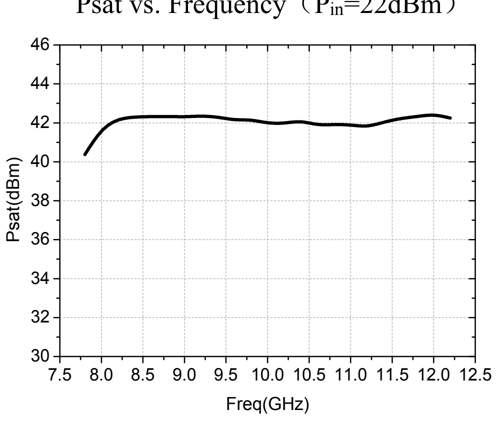
Note：1）The chip has been 100% on chip DC and RF tested.

Limited Rating Values

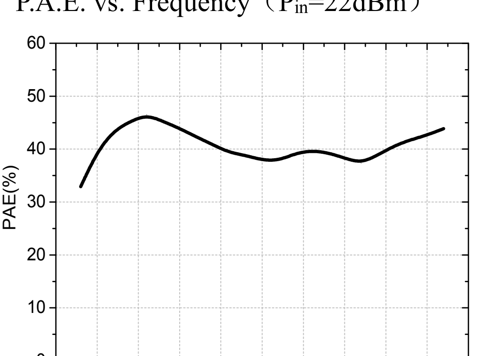
Parameter	Symbol	Value
Max. Drain Voltage	Vd	+35V
Min. Gate Voltage	Vg	-5V
Max. Input Power	Pin	+27dBm
Operating Temperature	T_{op}	-55℃～+125℃
Storage Temperature	T_{op}	-65℃～+150℃

Typical Testing Curves（Vd=+28V，Vg=-2.3V）

Psat vs. Frequency（P_{in}=22dBm）

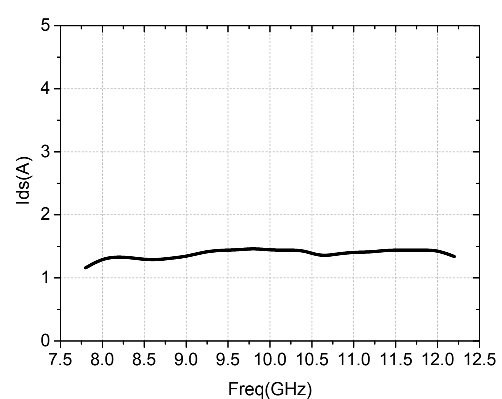
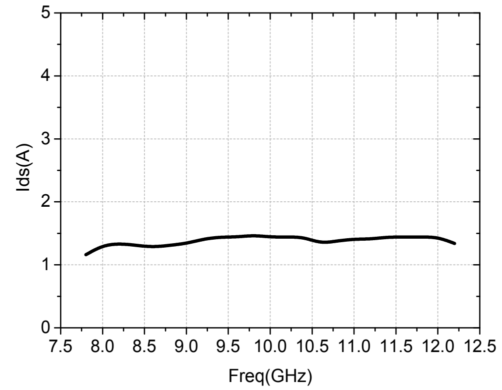


P.A.E. vs. Frequency（P_{in}=22dBm）

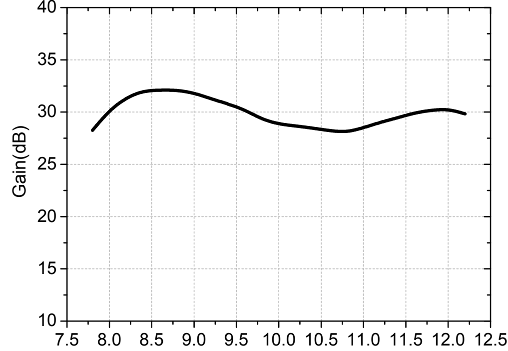


Power Gain vs. Frequency（P_{in}=22dBm）

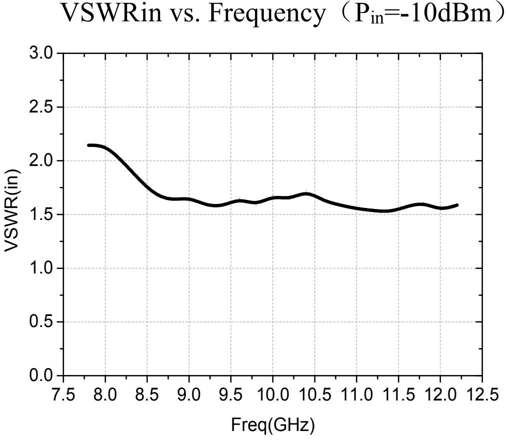
Dynamic Drain Current vs. Frequency（P_{in}=22dBm）

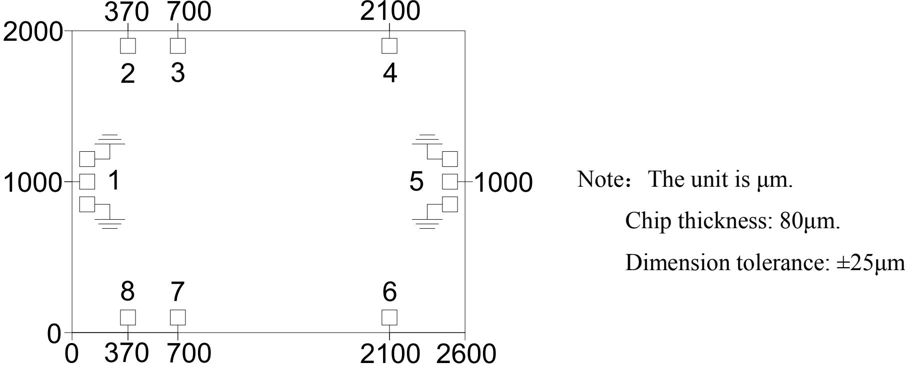
Small Signal Gain vs. Frequency（P_{in}=-10dBm）



VSWRin vs. Frequency（P_{in}=-10dBm）



Dimension and Outline



Note：The unit is µm.

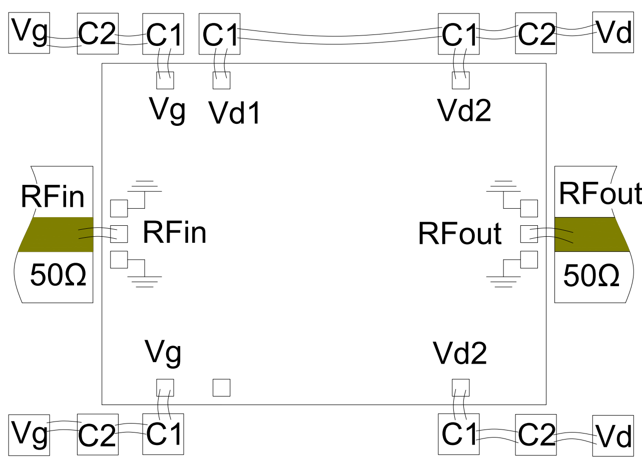
Chip thickness: 80µm.

Dimension tolerance: ±25µm.

Bonding Pad Definition

NO.	Symbol	Function	Size
1	RFin	RF signal input port, external 50 Ω system should be connected，blocking capacitor not needed.	100×100µm^2
2、8	Vg	Amplifier gate pad feed port，external 100pF、1000pF filter capacitors are needed.	100×100µm^2
3	Vd1	Amplifier drain pad feed port，external 100pF、1000pF filter capacitors are needed.	100×100µm^2
4、6	Vd2	Amplifier drain pad feed port，external 100pF、1000pF filter capacitors are needed.	100×100µm^2
5	RFout	RF signal output port, external 50 Ω system should be connected，blocking capacitor not needed.	100×100µm^2
7	GND	Grounding pad, only for testing	100×100µm^2

Assembly Diagram



Note：External capacitor C1=100pF，C2=1000pF

Features:

- Frequency: 14.5～16.5GHz
- Gain: 20dB
- Saturation Power output: 45dBm
- P.A.E: 30％
- +28V @ 1.5A（Quiescent）
- Dimension: 2.9mm×3.5mm×0.1mm

Electrical Specification（TA=+25℃, Vd=+28V, Vg=-1.8V）

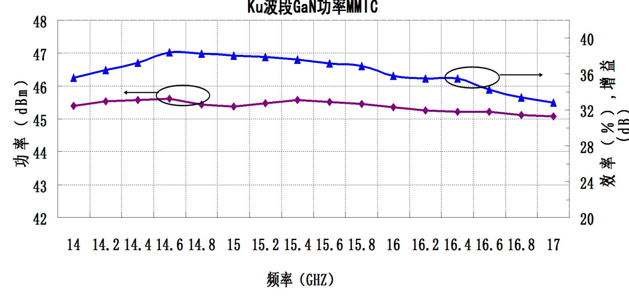
Parameter	Min	Typical	Max	Unit
Frequency	14.5-16.5			GHz
Power Gain	19	20	—	dB
Saturation Pout	45	45.2	—	dBm
P.A.E	30	35	—	%
Input VSWR	—	2.0	2.5	—
Dynamic Current	3			A

Note: 1)all chips have been 100% DC Tested
2) Testing condition: Vd=28V, Vg=-1.8V, P_{in}=24dBm, pulse width 100μs, 10% duty cycle

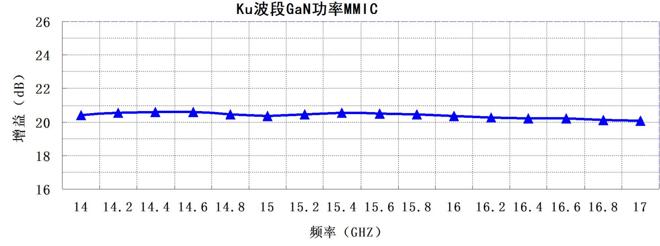
Limited Rating Values

Max Input Drain Voltage	+36V
Max Input Power	+30dBm
Storage Temperature	-65℃～+150℃
Operating Temperature	-55℃～+85℃

Testing Curves

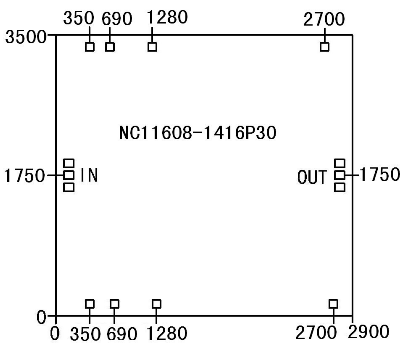


Psat /P.A.E VS Frequency



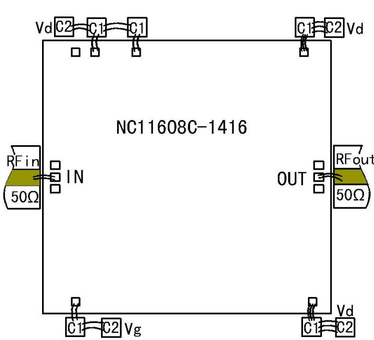
Power Gain VS Frequency

Dimension



Note: all units are um; input and output pad dimension 120×100um^2 ; biasing pad dimension 100×100um^2

Assembly Chart



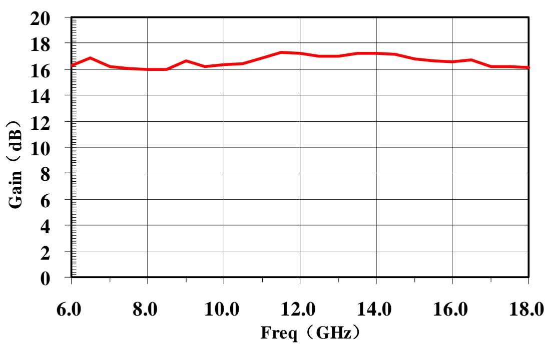
note: c=100pF, c2=0.01uF; 0.01μF filtering capacitor shall be applied to biasing gate ; diameter of golden wire 25um

Attention

1) 2 bonding wires should be used for input/output. The length of the wires should be shorter than 350μm.
2) Bonding with 80/20 Au/Sn. The temperature should be lower than 300℃ and the time should be less than 30 seconds.
3) Blocking capacitors in Input/Output are already integrated.
4) Antistatic protection should be taken.

Features

- Frequency：6GHz～18GHz
- Power Gain：17dB
- Psat：40dBm
- P.A.E.:20％
- +24V@1A(static)
- Chip Size：4.5mm×3.4mm×0.1mm



Electrical Specification（TA=+25℃, Vd=+24V，Vg=-2.2V）

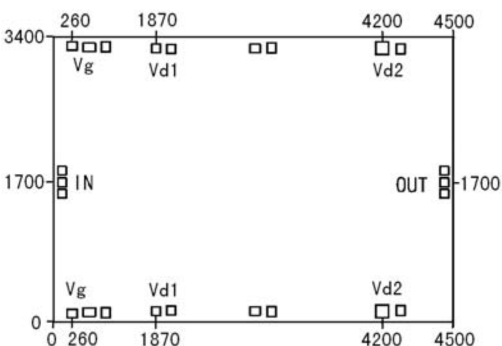
Parameter	Min.	Typ.	Max.	Unit
Frequency	6-18			GHz
Psat	40	40.5		dBm
P.A.E.	20	25		%
Power Gain	16	17		dB
VSWRin		2.5		-
Operating Current		2		A

Note：1）All chips have been on-chip 100% DC and RF tested .
2) RF Test Condition：Vd=+24V，Vg=-2.2V，CW.

More Temperature Testing Results can be provided upon Requested.

Dimensions and Outline

NC11609C-618P10 outline

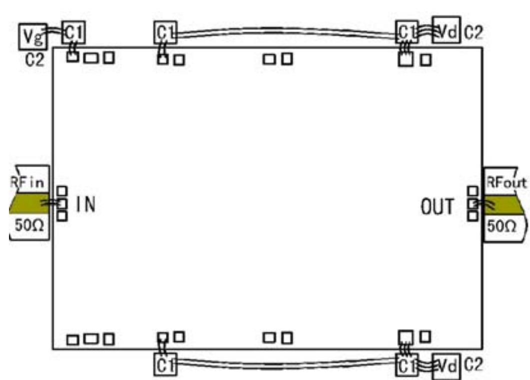


Note：The unit is um. Dimension of In/Out Pad 100×100μm².

Limited Rating Values

Max Input Vd	+28V
Max Input Power	+30dBm
Storage Temperature	-65℃～+150℃
Operating Temperature	-55℃～+125℃

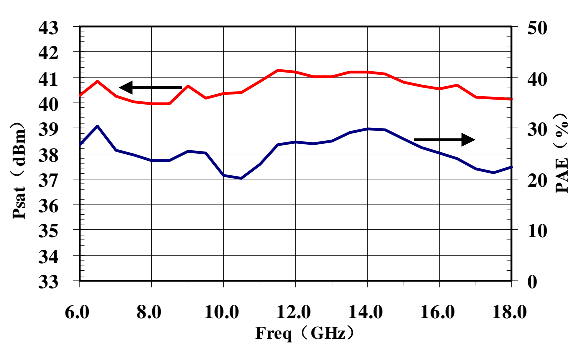
Assembly Diagram



Note：External capacitor c1=100pF,c2=0.01μF.
Diameter of bonding golden wire: 25μm.
Pay attention to heat dissipation when used in CW.

1)

Typical Testing Curves



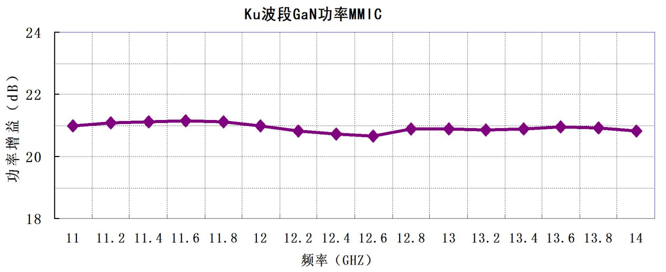
METDA Semiconductor

new NC11612C-1114P35V2

GaN MMIC Power Amplifier, 11GHz-14GHz

Features:

- Frequency: 11.0～14.0GHz
- Power Gain: 20.8dB
- Saturation Power: 45.8dBm
- P.A.E: 35％
- +28V @ 2.5A（Quiescent）
- Dimension: 4.0mm×4.1mm×0.1mm



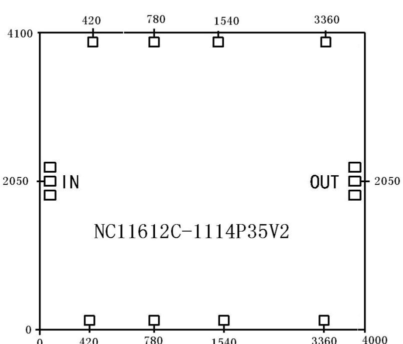
Power Gain VS Frequency

Electrical Specification（TA=+25℃,Vd=+28V，Vg=-1.8V）

Parameters	Min	Typical	Max	Unit
Frequency	11.0-14.0			GHz
Power Gain	20	20.8	—	dB
Saturation Pout	45.5	45.8	—	dBm
P.A.E	30	35	—	%
VSWR input	—	2.0	2.5	—
Dynamic Current	4			A

Note:1) all chips have been 100% DC tested.
2) Testing Condition: Vd=28V，Vg=-1.8V, P_{in}=25dBm，100µs pulse width，10% duty cycle

Dimension and Outline

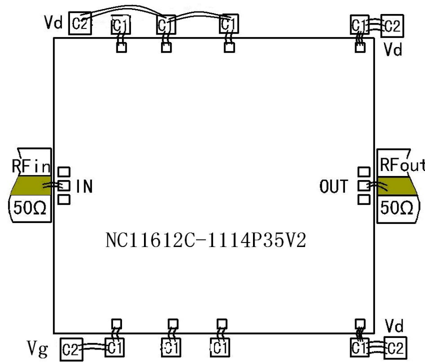


Note: all units are um; input and output pad dimension $100\times120um^2$, biasing pad dimension $100\times100um^2$

Limited Rating Value

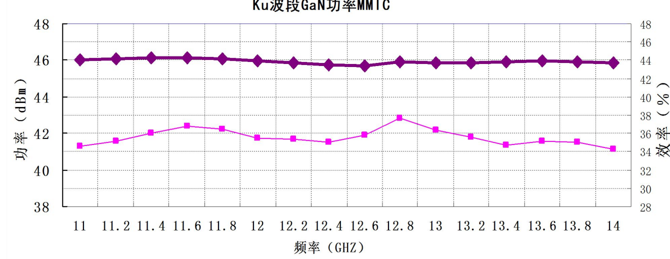
Max Input Vd	+30V
Max Input Power	+30dBm
Storage Temperature	-65℃～+150℃
Operation Temperature	-55℃～+85℃

Assembly Chart



note: external capacitor c1=100pF, c2=0.01uF（optional）; more than 0.01μF capacitor filter shall be applied on Gate biasing, diameter of bonding golden wire shall be 25um

Typical Testing Curves



Saturation Power output /Efficiency VS Frequency

Attention

1) 2 bonding wires should be used for input/output. The length of the wires should be shorter than 350μm.
2) Bonding with 80/20 Au/Sn. The temperature should be lower than 300℃ and the time should be less than 30 seconds.
3) Blocking capacitors in Input/Output are already integrated.
4) Antistatic protection should be taken.

NC11613C-1618P30
GaN MMIC Power Amplifier, 16GHz-18GHz

Features

- Frequency：16GHz～18GHz
- Power Gain：20dB
- Psat：45dBm
- P.A.E：30％
- +28V @ 2.5A（quiescent state）
- Chip Size：3.7mm×3.6mm×0.1mm

Electrical Specification（TA=+25℃,Vd=+28V，Vg=-2.0V）

Parameter	Min	Typ.	Max	Unit
Frequency	16-18			GHz
Power Gain	19	20	—	dB
Saturation Pout	44.8	45.2	—	dBm
P.A.E	30	33	—	%
VSWRin	—	2.0	2.5	—
Dynamic Current	4			A

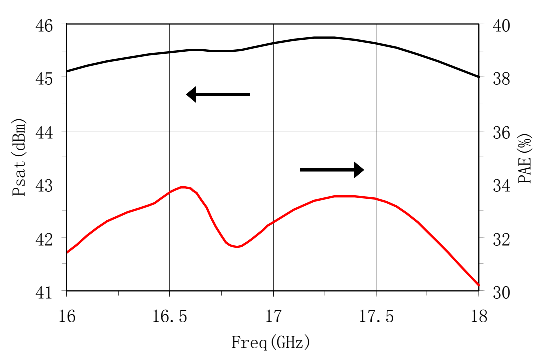
Note：1) All chips have been 100% DC tested.
2) Test condition：Vd=+28V，Vg=-2.0V, pulse width 100μs，duty cycle 10%，P_{in}=25dBm

Limited Rating Values

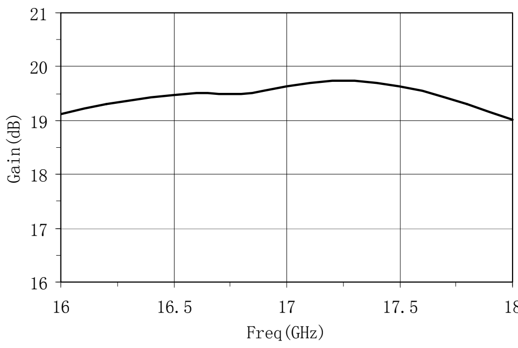
Max Input Vd	+30V
Max Input Power	+30dBm
Storage Temperature	-65℃～+150℃
Operation Temperature	-55℃～+85℃

Typical Testing Curves

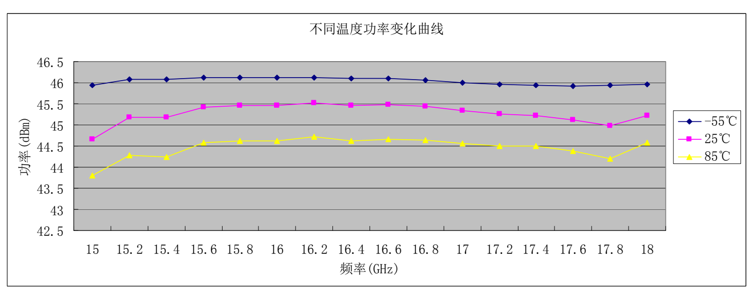
Psat/Efficiency vs. Frequency



Power Gain vs. Frequency



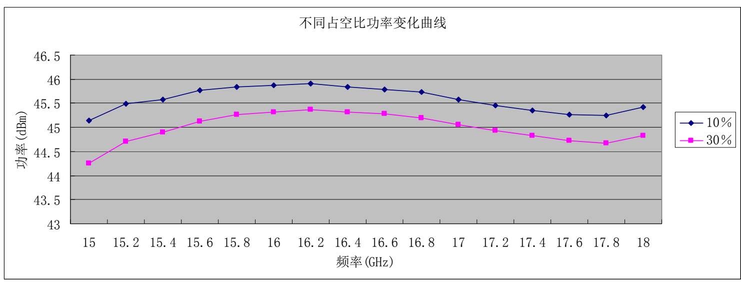
Pout VS. Temperature



Power vs Frequency Curves under different temperature range

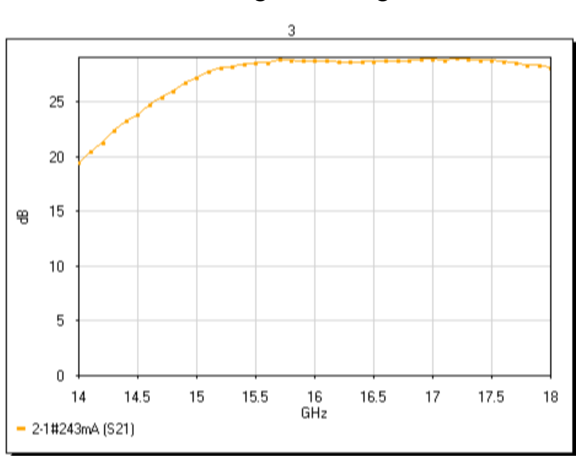
（V_{DS}=28V,V_{GS}=-2V，Duty Cycle 10%，Pulse width 100us）

Power vs Frequency Curves under different Duty Cycle

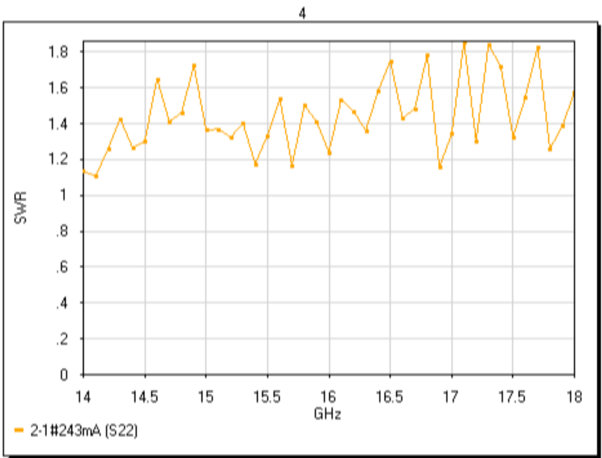


（V_{DS}=28V,V_{GS}=-1.8V）

Small Signal Testing Result:

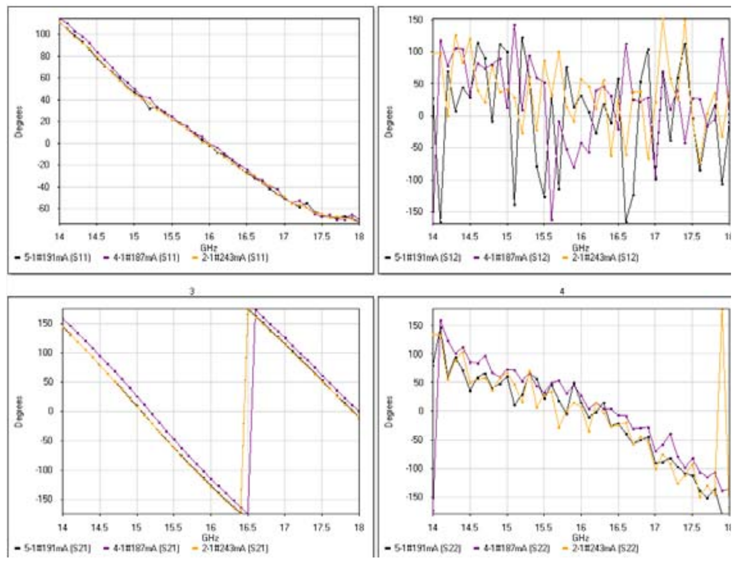


Small Signal Gain S21，（V_{DS}=28V,V_{GS}=-2V）



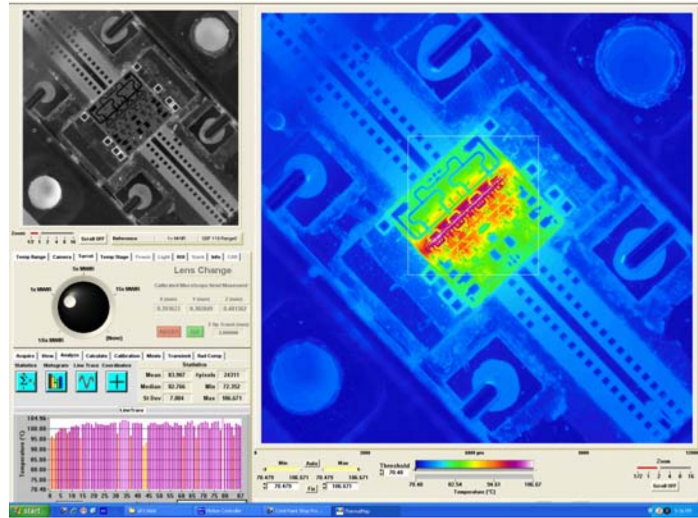
VSWRin，（V_{DS}=28V,V_{GS}=-2V）

VSWRout，（V_{DS}=28V,V_{GS}=-2V）

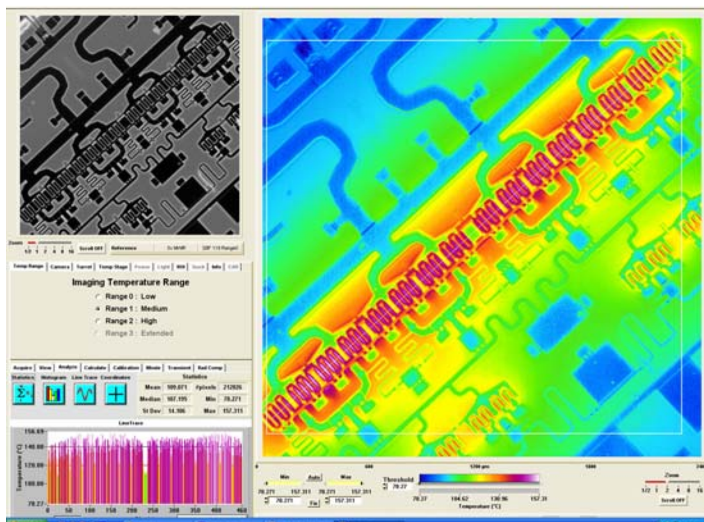


Phase Characteristics，（V_{DS}=28V,V_{GS}=-2V）

Thermal Resistance Characteristics



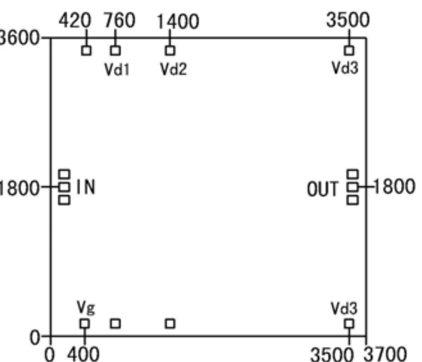
1X Pixel Thermal spread（V_{DS}=28V,I_{DS}=0.8A）



5X Pixel Thermal spread（V_{DS}=28V,I_{DS}=1.4A）

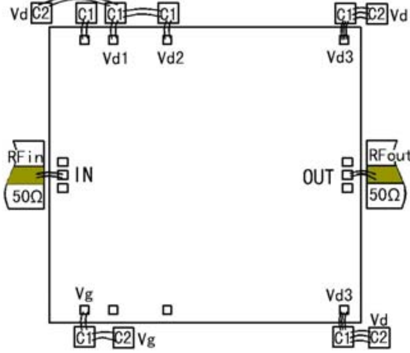
The thermal resistance is less than 3℃/W, and the power variation between high/low temperature is 1.5 dB, the power output will be dropped by 0.5 dB under 30% duty cycle.

Dimension and Outline



Note： The unit is μm. Input and output pad dimension: 100×120μm^2.
Bias pad dimension:100×100μm^2

Assembly Diagram



Note：External capacitor c=100pF,c2=0.01μF. A 0.01μF capacitor filter is needed for gate bias. Diameter of bonding gold wires: 25μm.

Attention:

1) Two bonding wires are needed for input and output. The length should be shorter than 350μm.

2)Bonding with 80/20 Au/Sn. The temperature should be lower than 300 ℃ and the time should be less than 30 seconds.

3)Blocking capacitors in Input/Output are already integrated.

GaN MMIC Power Amplifier，33GHz-35GHz

Features

- Frequency：33GHz～35GHz
- Power Gain：15dB
- Psat：38dBm
- P.A.E：18%
- +22V @ 1.5A（Quiescent）
- Dimension：3.65mm×2.55mm×0.10mm

Electrical Specification

（TA=+25℃, Vd=+22V，Vg=-1.8V）

Parameter	Min	Typ.	Max.	Unit
Frequency		33-35		GHz
Psat		38		dBm
Power Gain		15		dB
P.A.E		18		%
Dynamic Operating Current		1.5		A

Note：1) All chips have been 100% DC tested.

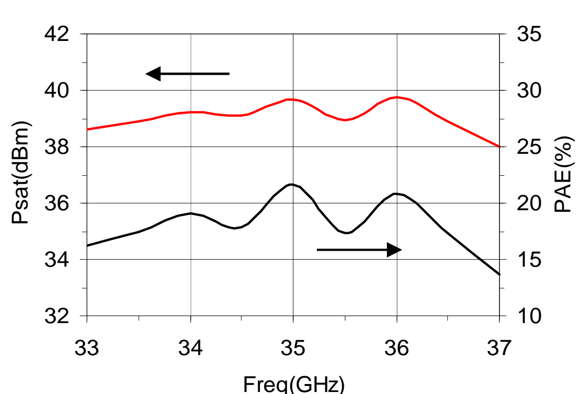
2) Test Condition：Vd=+22V，Vg=-1.8V，P_{in}=24dBm，pulse width 100μs，duty cycle 2%.

Limited Rating Values

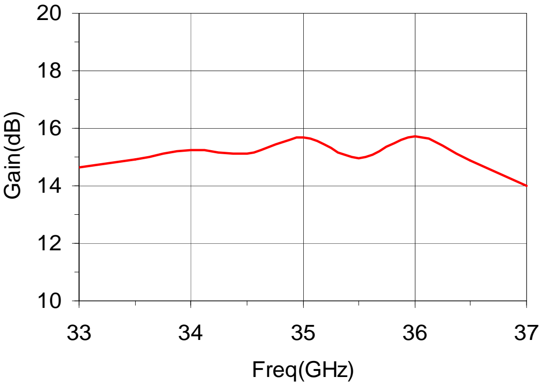
Vds	+24V
Vgs	-6V
Input CW Power	+30dBm
Channel Temperature	+175℃
Storage Temperature	-65℃～+150℃

Typical Testing Curves

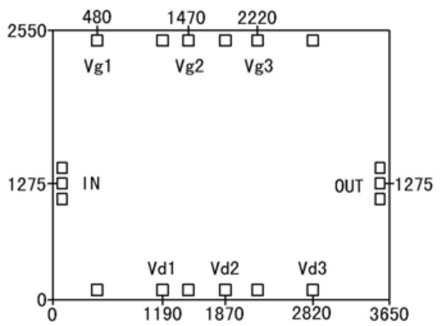
Psat/Efficiency vs. Frequency



Power Gain vs. Efficiency



Dimension and Outline

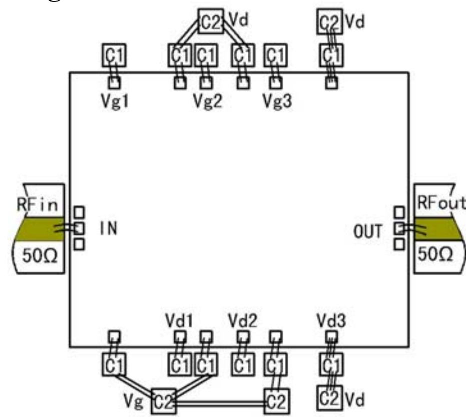


Note：The unit is μm.

Dimension of input and output pad: 100×120μm^2.

Dimension of bias pad 120×120μm^2

Assembly Diagram



Note：External capacitor C1:100pF，C2:1000pF

Attention

1) Two bonding wires are needed for input and output(diameter 25μm). Bonding wires shall not be longer than 500μm.

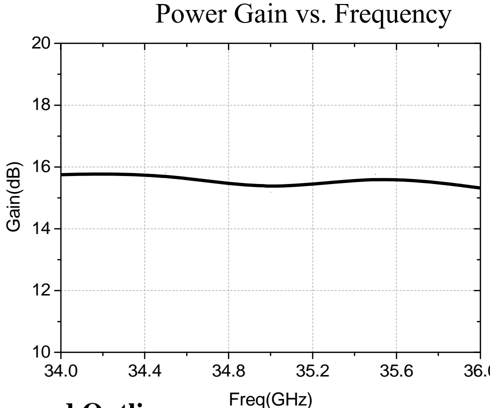
2)Bonding with 80/20 Au/Sn. Temperature should be lower than 300℃ and time should be less than 30 seconds.

3)Blocking capacitors in Input/Output are already integrated.

GaN MMIC Power Amplifier，34GHz-36GHz

Features:

- Frequency：34GHz～36GHz
- Power Gain：15.5dB
- Psat：41.5dBm
- P.A.E：20%
- +22V @ 3A（Quiescent）
- Chip Size：5.05mm×4.84mm×0.10mm



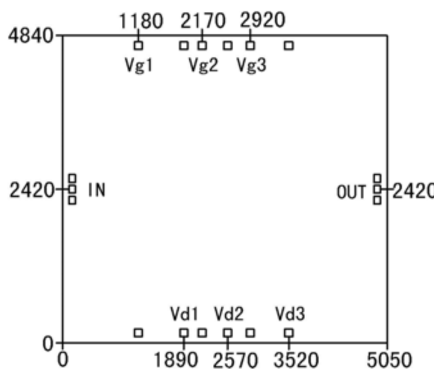
Electrical Specification（TA=+25℃, Vd=+22V, Vg=-1.8V）

Parameter	Min.	Typ.	Max	Unit
Frequency	34-36			GHz
Psat		41.5		dBm
Power Gain		15.5		dB
P.A.E		20		%
Dynamic Operating Current	3.2			A

Note：1) All chips have been 100% DC tested.

2) Test condition：Vd=+22V，Vg=-1.8V，P_{in}=26dBm,，pulse width 100μs，duty cycle 2%.

Dimension and Outline



Note：The unit is μm.

Input and output pad dimension: 100×120μm².

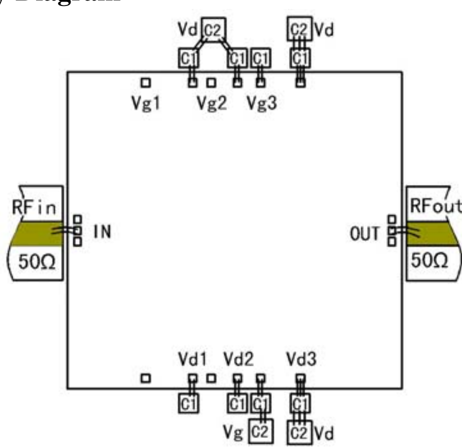
Bonding pad dimension:120×120μm²；

Tolerance of outline dimensions：±50μm。

Limited Rating Values

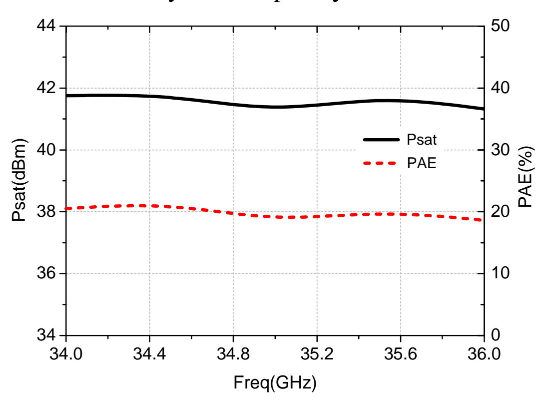
Vds	+24V
Vgs	-6V
Input CW Power	+30dBm
Channel Temperature	+175℃
Storage Temperature	-65℃～+150℃

Assembly Diagram



Note：External capacitor C1:100pF，C2:1000pF。

Typical Testing Curves



Attention

1) Two bonding wires are needed for input and output(diameter: 25μm). Bonding wires shall not be longer than 500μm.

2)Bonding with 80/20 Au/Sn. Temperature should be lower than 300℃ and time should be less than 30 seconds.

3)Blocking capacitors in Input/Output are already integrated.

METDA Semiconductor

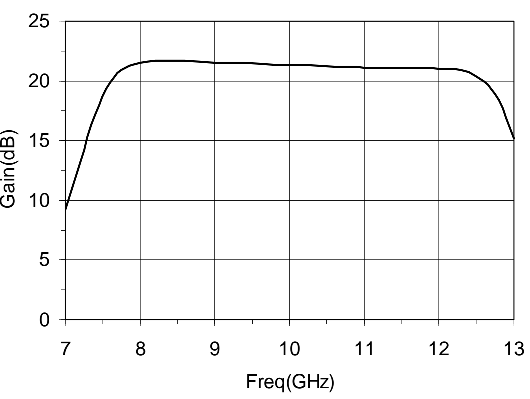
NC11619C-812P50

GaN MMIC Power Amplifier, 8GHz-12GHz

Features

- Frequency：8GHz～12GHz
- Power Gain：23dB
- Psat：47dBm
- P.A.E：40%
- +28V@2A(Quiescent)
- Chip Size：4.8mm×5.3mm×0.1mm

Power Gain vs. Frequency



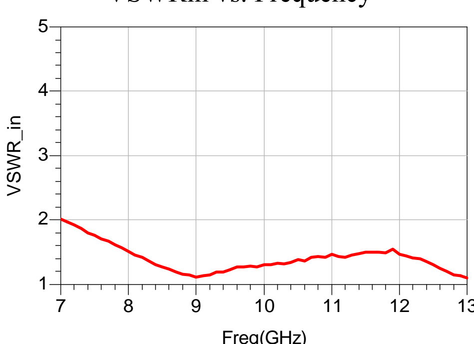
Electrical Specification（TA=+25℃，Vg=-2V，Vd=+28V ）

Parameter	Min.	Typ.	Max.	Unit
Frequency	8-12			GHz
Psat	47	47.3	47.5	dBm
Power Gain		23		dB
Gain Flatness			±0.25	dB
P.A.E	40			%
VSWRin			2.0	-
Operating Current		4.5		A

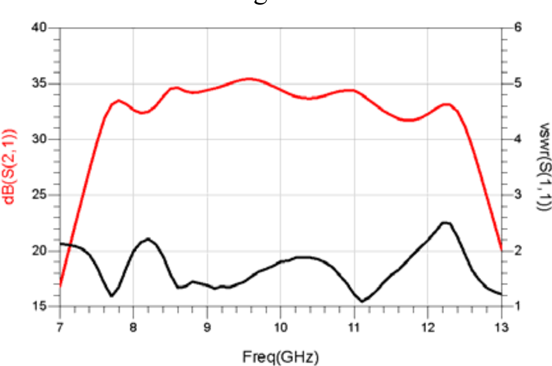
Note：1）All chips have been 100% DC and RF tested.

2）Test Condition：Vd=+28V，Vg=-2V，P_{in}=24dBm，pulse width 2ms， duty cycle 30%.

VSWRin vs. Frequency



Small Signal Features



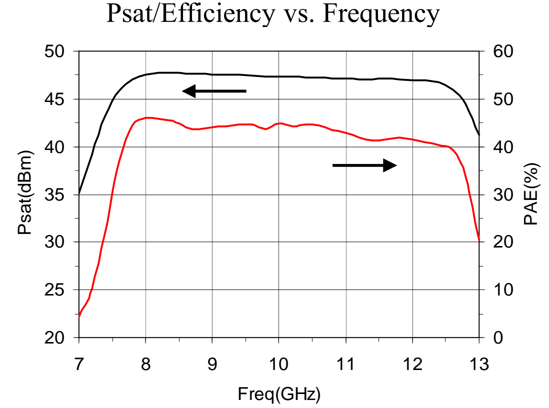
Testing Condition：28V/-2V，Input Pin=-20dBm

Limited Rating Values

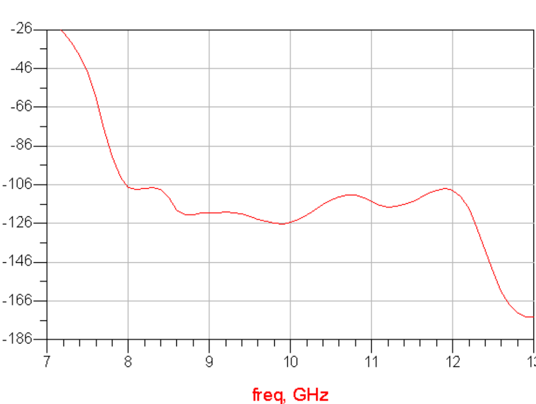
Parameters	Values
VDS	+40V
VGS	-6V
Input CW Power	+35dBm
Channel Temperature	+175℃
Storage Temperature	-65℃～+150℃

Typical Testing Curves

Psat/Efficiency vs. Frequency



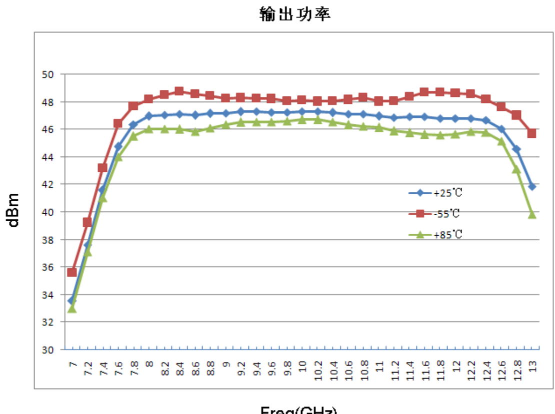
Phase Linearity：8-12GHz In band ±10°

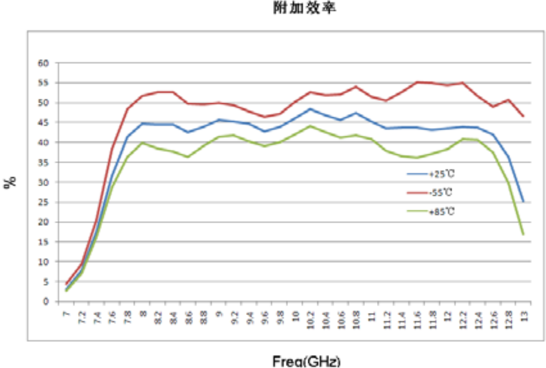


Testing Condition：28V/-2V，Input Pin=-20dBm

Spectrum in Low and High Temperature/ Power Variation

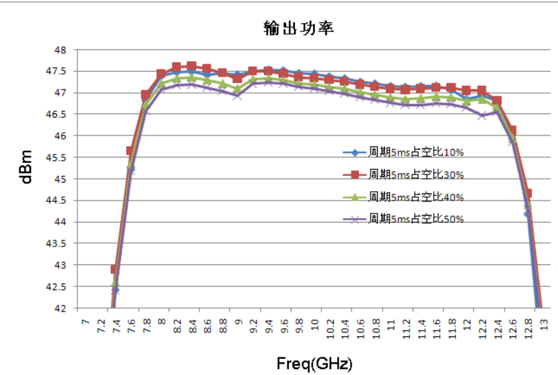
Operating Temperature：-55℃ ~ +85℃，spectrum of high and low temperature are all normal without self oscillation

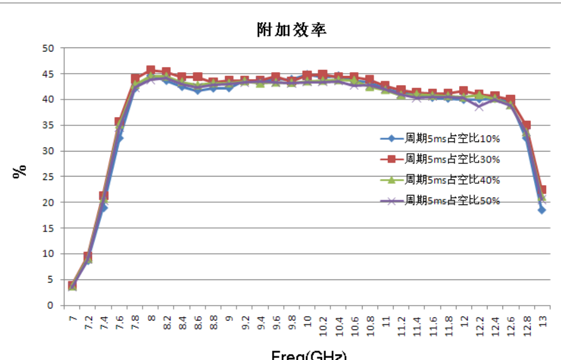




Testing Condition：fixed input power Pin=26dBm

Power Change upon Duty Cycle

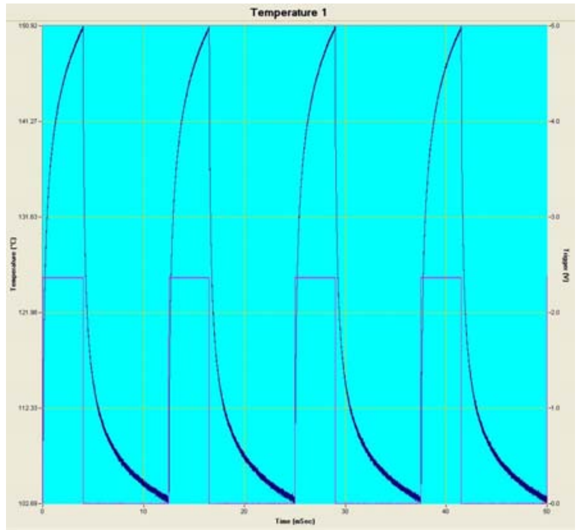




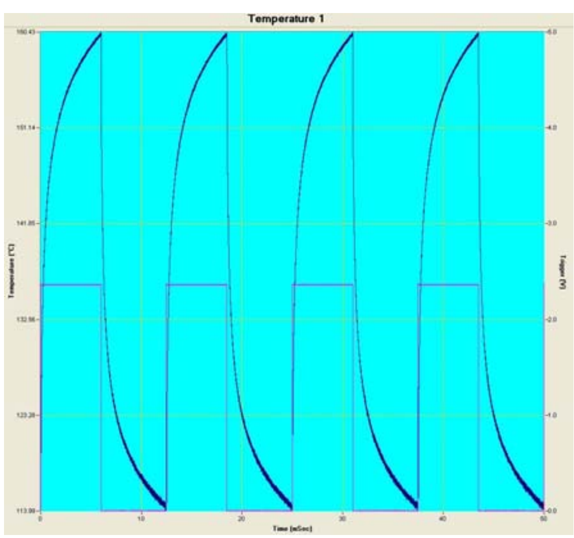
Testing Condition：fixed input power Pin=26dBm，Drain Pulse Modulation, set period of 5 ms without change, change the duty cycle

Channel temperature testing result：

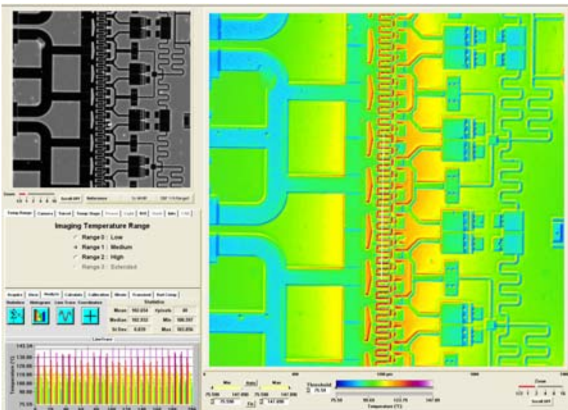
Testing Condition 1： Drain Pulse Modulation Signal, length 12ms，pulse width 4ms，peak voltage and current as 28V/2.7A（peak thermal dissipation 75W，average thermal dissipation 25W），environmental temperature 70℃，peak channel temperature 150℃



Testing Condition 2： Drain Pulse Modulation Signal, length 12ms，pulse width 6 ms， peak voltage and current as 28V/2.7A（peak thermal dissipation 75W，average thermal dissipation 37.5 W），environmental temperature 70℃，peak channel temperature 160℃



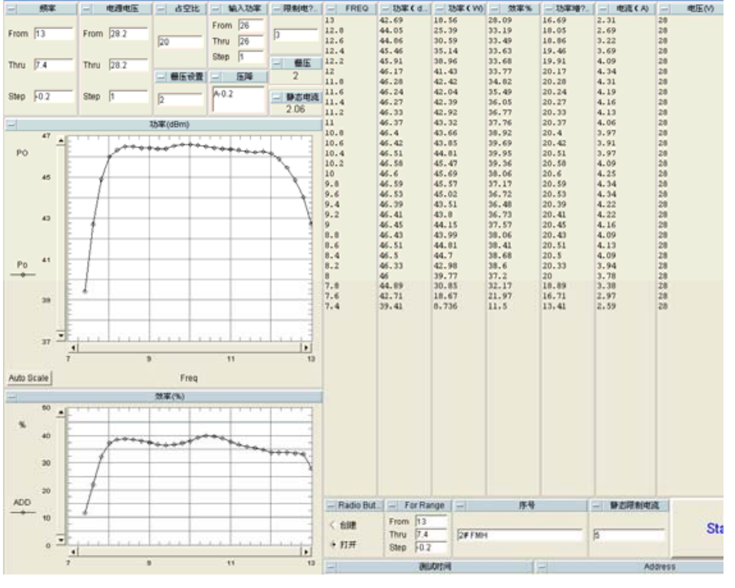
Testing Condition 3: DC 28V/0.81A（thermal dissipation 23W）, environmental temperature 70℃，Channel temperature 148℃，Equal DC thermal resistance 3.4℃/W



It is the temperature drawing of chip center area

Packaged Test Result

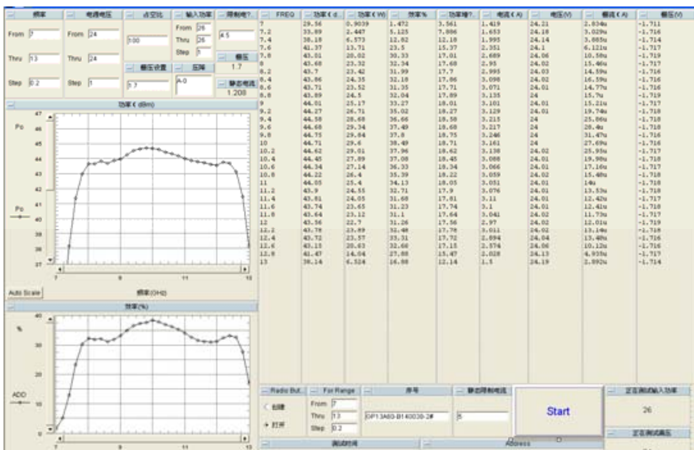
Test result with metal ceramic package(including losses of jigs, etc.). Period: 5ms，duty cycle: 30%



Derate CW Test Result

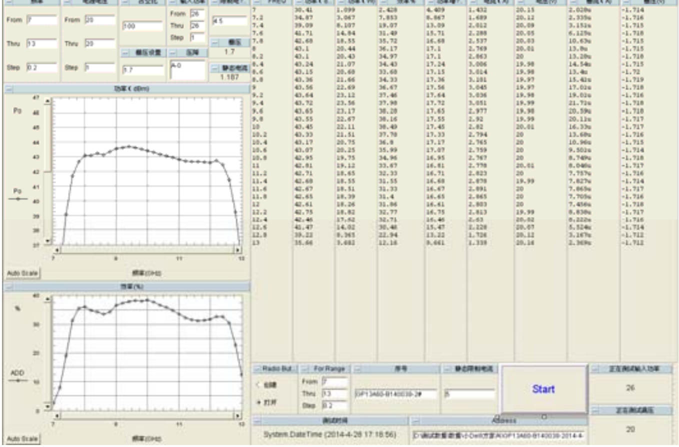
CW，Operating voltage: 24V、22V、20V

Operating voltage: 24V

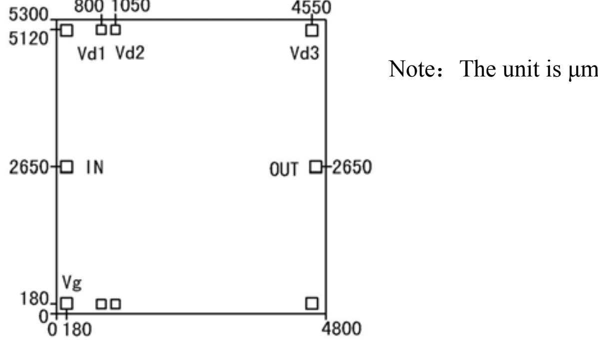


Operating voltage 22V

Operating voltage :20V

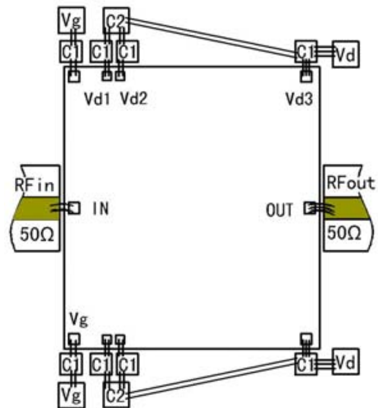


Dimension and Outline



Note：The unit is μm.

Assembly Diagram



Note：External Capacitor C1=100pF，C2=1000pF

Attention：

1) Gold wires (diameter: 25μm～30μm) are suggested for bonding. The temperature of bonding platform shall not exceed 250℃.

2) Bonding with 80/20 Au/Sn. Temperature should be lower than 300℃ and time should be less than 30 seconds.

3)Blocking capacitors in Input/Output are already integrated.

Features

- Frequency：8GHz～12GHz
- Power Gain：22dB
- Psat：47dBm
- P.A.E：40%
- +28V@2A(Quiescent)
- Chip Size：4.8mm×5.3mm×0.1mm

Power Gain vs. Frequency

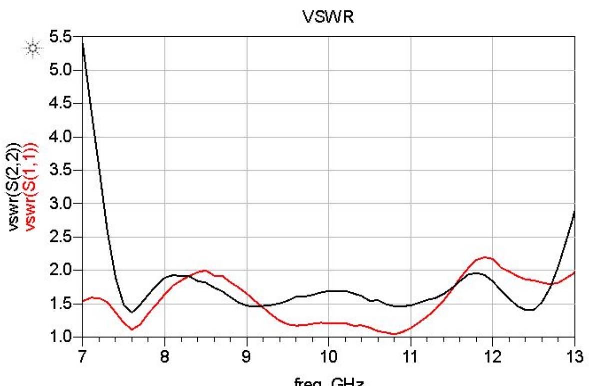
Electrical Specification（TA=+25℃，Vg=-2V，Vd=+28V ）

Parameter	Min.	Typ.	Max.	Unit
Frequency	8-12			GHz
Psat	47	47.3	47.5	dBm
Power Gain		22		dB
Gain Flatness			±0.25	dB
P.A.E	40			%
VSWRin			2.0	-
Operating Current		4.5		A

Note： 1）All chips have been 100% DC and RF tested.

2）Test Condition：Vd=+28V，Vg=-2.2V，P_{in}=25dBm，pulse width 2ms， duty cycle 30%.

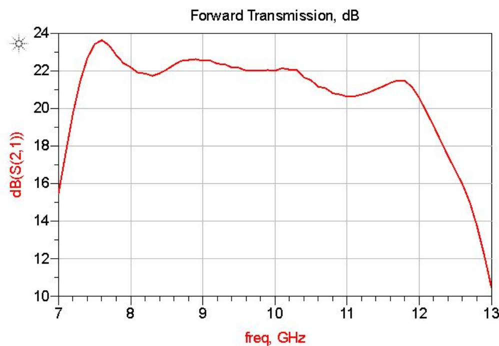
VSWRin vs. Frequency



Limited Rating Values

Parameters	Values
VDS	+40V
VGS	-6V
Input CW Power	+35dBm
Channel Temperature	+175℃
Storage Temperature	-65℃～+150℃

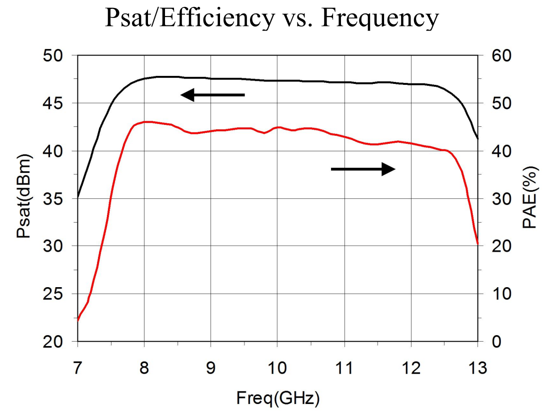
Small Signal Features



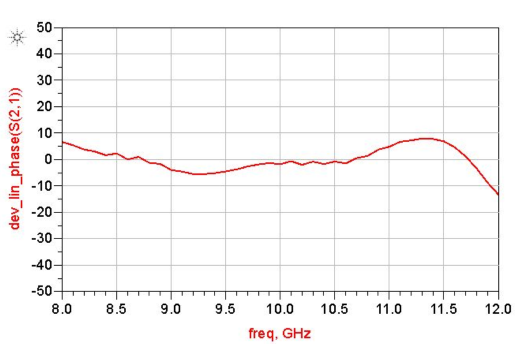
Testing Condition：28V/-2.2V，Input Pin=-20dBm

Typical Testing Curves

Psat/Efficiency vs. Frequency



Phase Linearity：8-12GHz In band ±10°



Testing Condition：28V/-2V，Input Pin=-20dBm

Spectrum in Low and High Temperature/ Power Variation

Operating Temperature：-55℃ ~ +85℃，spectrum of high and low temperature are all normal without self oscillation

输出功率

dBm

+25℃
-55℃
+85℃

Freq(GHz)

附加效率

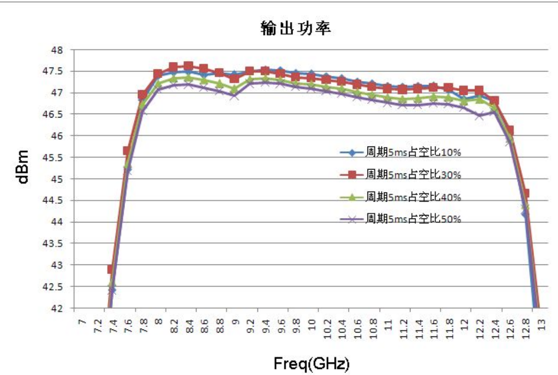
%

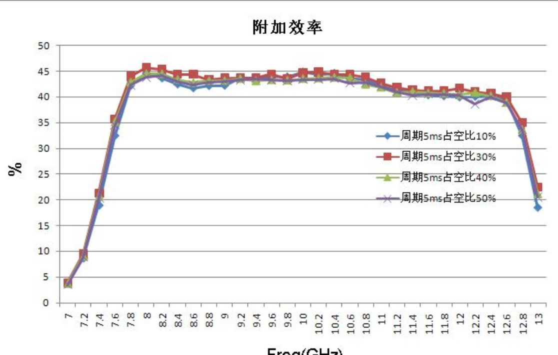
+25℃
-55℃
+85℃

Freq(GHz)

Testing Condition：fixed input power Pin=26dBm

Power Change upon Duty Cycle

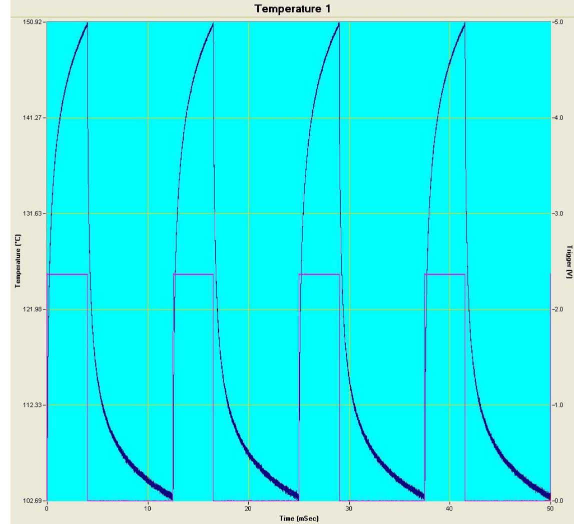




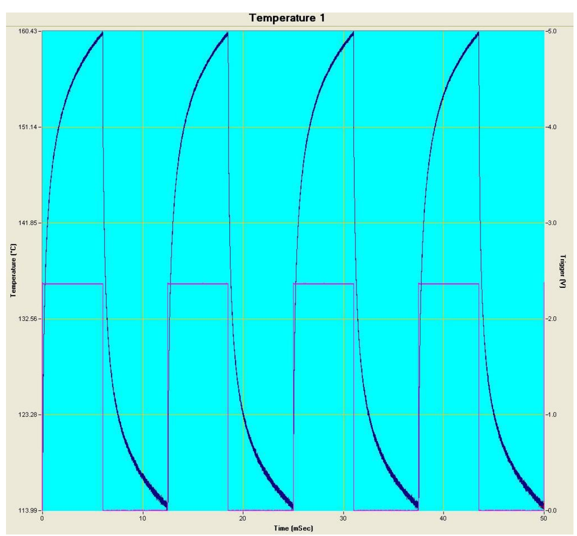
Testing Condition：fixed input power Pin=26dBm，Drain Pulse Modulation, set period of 5 ms without change, change the duty cycle

Channel temperature testing result：

Testing Condition 1： Drain Pulse Modulation Signal, length 12ms，pulse width 4ms，peak voltage and current as 28V/2.7A（peak thermal dissipation 75W，average thermal dissipation 25W），environmental temperature 70℃，peak channel temperature 150℃



Testing Condition 2： Drain Pulse Modulation Signal, length 12ms，pulse width 6 ms，peak voltage and current as 28V/2.7A（peak thermal dissipation 75W，average thermal dissipation 37.5 W），environmental temperature 70℃，peak channel temperature 160℃



Testing Condition 3: DC 28V/0.81A（thermal dissipation 23W）, environmental temperature 70℃，Channel temperature 148℃，Equal DC thermal resistance 3.4℃/W

It is the temperature drawing of chip center area

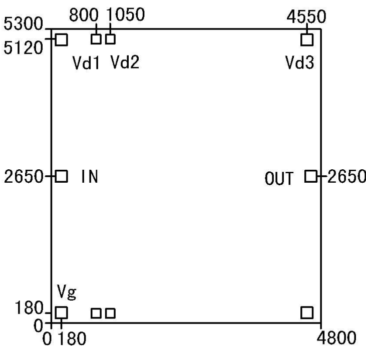
Attention：

1) Gold wires (diameter: 25μm～30μm) are suggested for bonding. The temperature of bonding platform shall not exceed 250℃.

2) Bonding with 80/20 Au/Sn. Temperature should be lower than 300℃ and time should be less than 30 seconds.

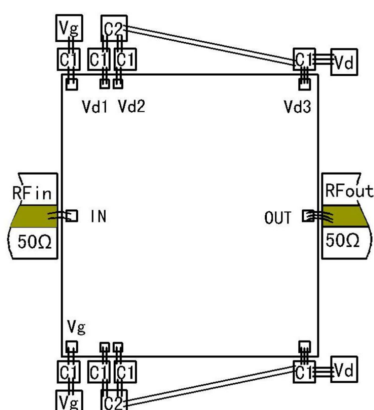
3)Blocking capacitors in Input/Output are already integrated.

Dimension and Outline



Note：The unit is μm.

Assembly Diagram



Note：External Capacitor C1=100pF，C2=1000pF

Features

- Frequency：8GHz～12GHz
- Power Gain：23dB
- Psat：47dBm
- P.A.E：40%
- +28V@2A(Quiescent)
- Chip Size：4.8mm×5.3mm×0.1mm

Power Gain vs. Frequency

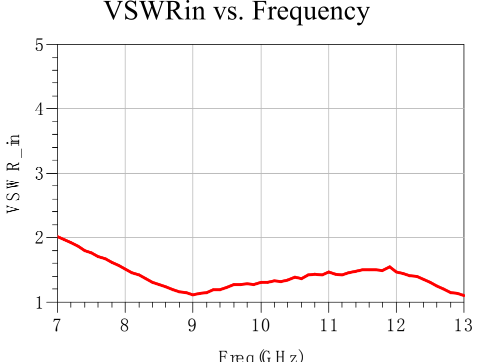
Electrical Specification（TA=+25℃，Vg=-2V，Vd=+28V ）

Parameter	Min.	Typ.	Max.	Unit
Frequency		8-12		GHz
Psat	47	47.3	47.5	dBm
Power Gain		23		dB
Gain Flatness			±0.25	dB
P.A.E	40			%
VSWRin			2.0	-
Operating Current		4.5		A

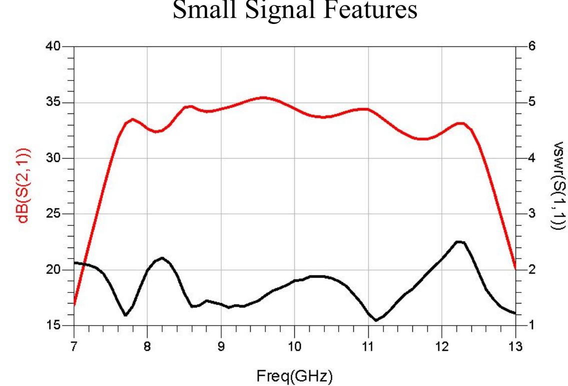
Note： 1） All chips have been 100% DC and RF tested.

2）Test Condition：Vd=+28V，Vg=-2V，P_{in}=24dBm，pulse width 2ms， duty cycle 30%.

VSWRin vs. Frequency



Small Signal Features



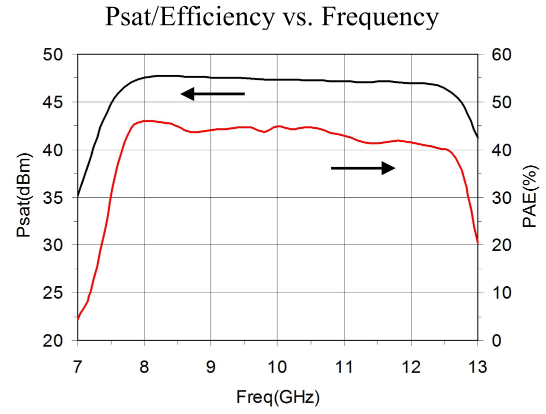
Testing Condition：28V/-2V，Input Pin=-20dBm

Limited Rating Values

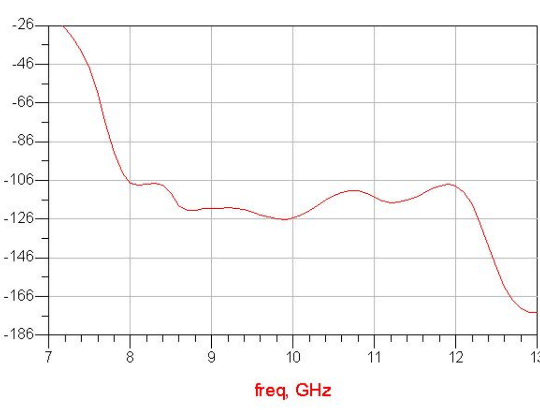
Parameters	Values
VDS	+40V
VGS	-6V
Input CW Power	+35dBm
Channel Temperature	+175℃
Storage Temperature	-65℃～+150℃

Typical Testing Curves

Psat/Efficiency vs. Frequency



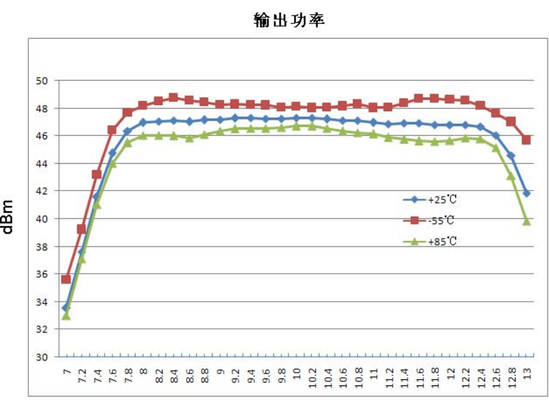
Phase Linearity：8-12GHz In band ±10°

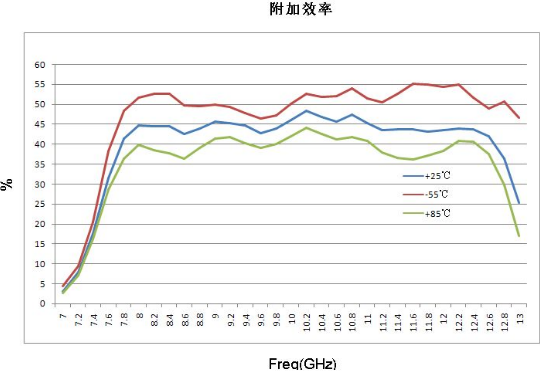


Testing Condition：28V/-2V，Input Pin=-20dBm

Spectrum in Low and High Temperature/ Power Variation

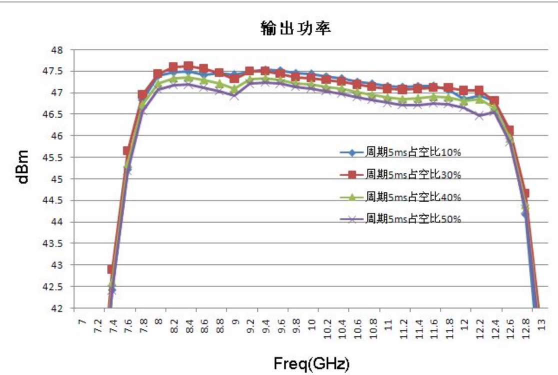
Operating Temperature：-55℃ ~ +85℃，spectrum of high and low temperature are all normal without self oscillation

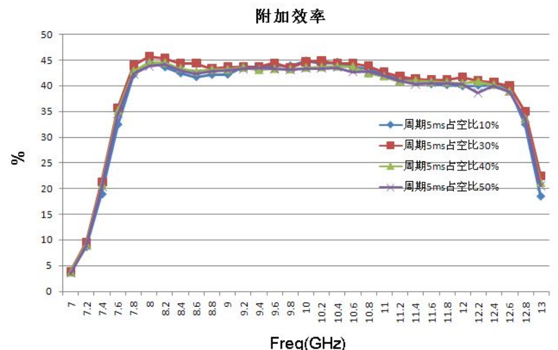




Testing Condition：fixed input power Pin=26dBm

Power Change upon Duty Cycle

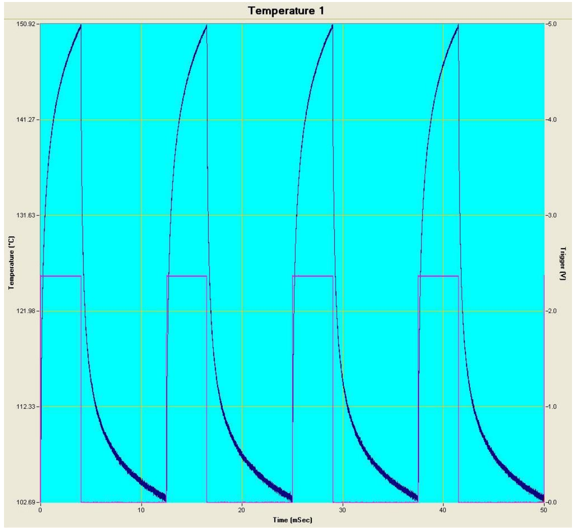




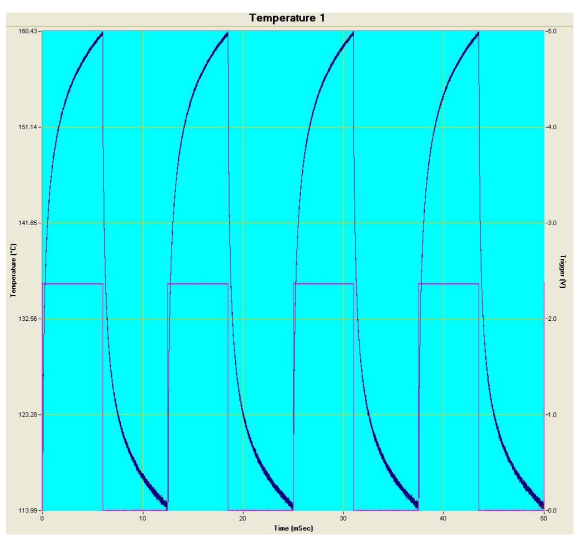
Testing Condition：fixed input power Pin=26dBm，Drain Pulse Modulation, set period of 5 ms without change, change the duty cycle

Channel temperature testing result：

Testing Condition 1： Drain Pulse Modulation Signal, length 12ms，pulse width 4ms，peak voltage and current as 28V/2.7A（peak thermal dissipation 75W，average thermal dissipation 25W），environmental temperature 70℃，peak channel temperature 150℃



Testing Condition 2： Drain Pulse Modulation Signal, length 12ms，pulse width 6 ms，peak voltage and current as 28V/2.7A（peak thermal dissipation 75W，average thermal dissipation 37.5 W），environmental temperature 70℃，peak channel temperature 160℃



Testing Condition 3: DC 28V/0.81A（thermal dissipation 23W），environmental temperature 70℃，Channel temperature 148℃，Equal DC thermal resistance 3.4℃/W

It is the temperature drawing of chip center area

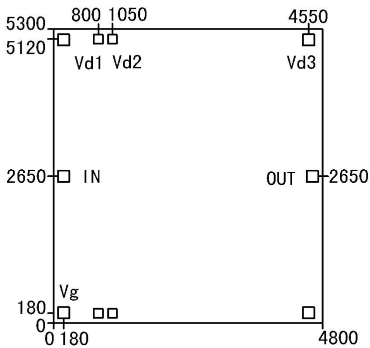
Attention：

1) Gold wires (diameter: 25μm～30μm) are suggested for bonding. The temperature of bonding platform shall not exceed 250℃.

2) Bonding with 80/20 Au/Sn. Temperature should be lower than 300℃ and time should be less than 30 seconds.

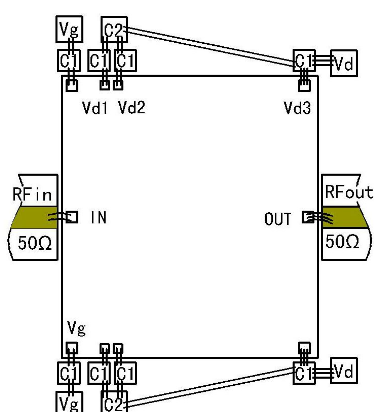
3)Blocking capacitors in Input/Output are already integrated.

Dimension and Outline



Note：The unit is μm.

Assembly Diagram

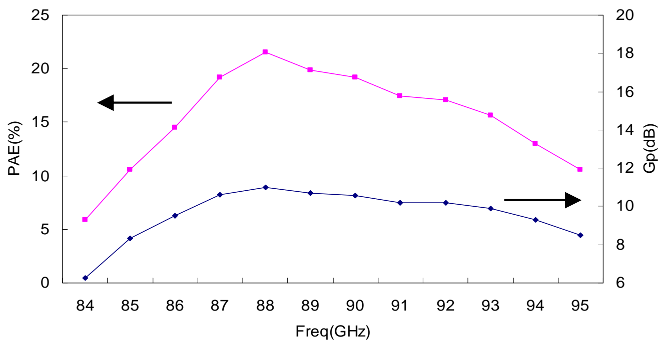


Note：External Capacitor C1=100pF，C2=1000pF

Features

- Frequency：90GHz～95GHz
- Linear Gain：12dB
- Psat：27dBm
- +15V@0.3A
- Chip Size：3.42mm×1.40mm×0.05mm

P.A.E./Power Gain vs. Frequency

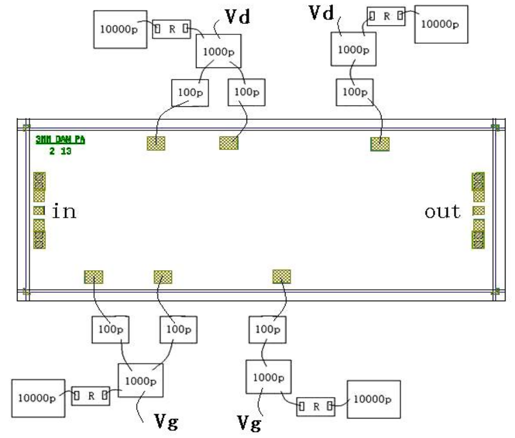


Electrical Specification（TA=+25℃, Vd=+15V, Vg=-2.2V）

Parameter	Min.	Typ.	Max.	Unit
Frequency	90-95			GHz
Psat	27			dBm
Power Gain	8			dB
VSWRin/out			3:1	-
Operating Current		300		mA

Note：1) RF Test Condition：Vd=+15V，Vg=-2.2V，P_{in}=19dBm，CW

Assembly Diagram

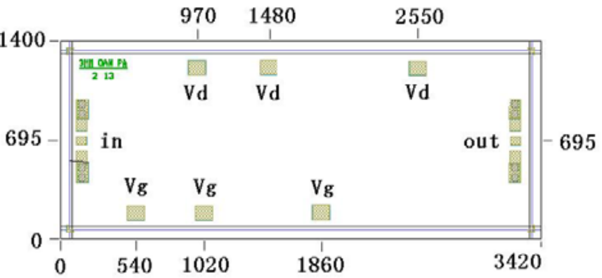


Note：R=10Ω

Limited Rating Values

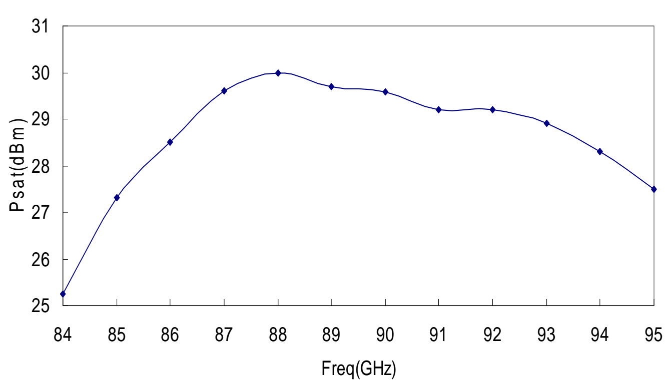
Max. Vds	+18V
Min. Vgs	-5V
Max. Input Power	+21dBm
Operating Temperature	-55℃～+125℃
Storage Temperature	-65℃～+150℃

Dimensions and Outline



Typical Testing Curves

Psat vs. Frequency



Attention

1） Gold wires (diameter: 25μm～30μm) are suggested to be used. The temperature of bonding platform should not exceed 250℃.

2） Antistatic protection should be taken.

Features

- Frequency：14GHz～18GHz
- Power Gain：17.5dB
- Saturation Power output：42.5dBm
- P.A.E：37%
- +28V@0.65A(Quiescent)
- Chip Dimension：3.00mm×2.10mm×0.08mm

Electrical Specification（TA=+25℃，Vg=-2V，Vd=+28V ）

Parameter	Min	Typical	Max	Unit
Frequency		14-18		GHz
Saturation Pout	42	42.5	42.8	dBm
Power Gain		17.5		dB
Gain Flatness			±0. 4	dB
P.A.E	37			%
VSWR in			2.0	-
Operation Current		1.6	1.7	A

Note：1）All units have been 100% DC tested and RF tested.

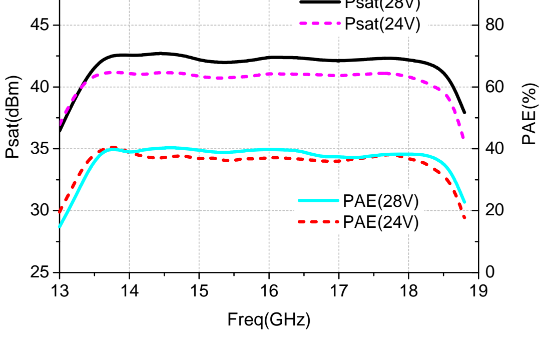
2）Testing Condition：Vd=+28V，Vg=-2V，P_{in}=25dBm，Pulse width：1ms，Duty Cycle：20%。

Limited Rating Value

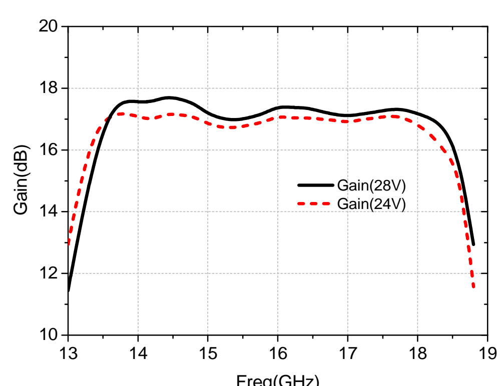
Parameter	Value
Vds	+40V
Vgs	-6V
Max Input CW Power	+35dBm
Junction Temperature	+200℃
Storage Temperature	-65℃～+150℃

Typical Testing Curves

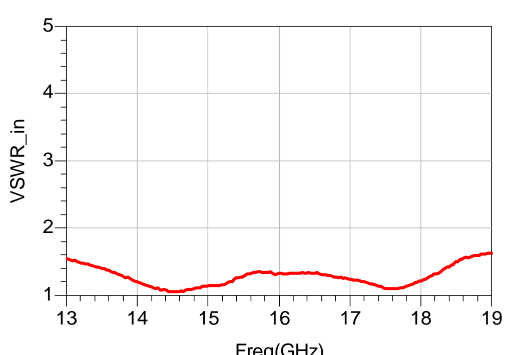
Psat/P.A.E vs. Frequency



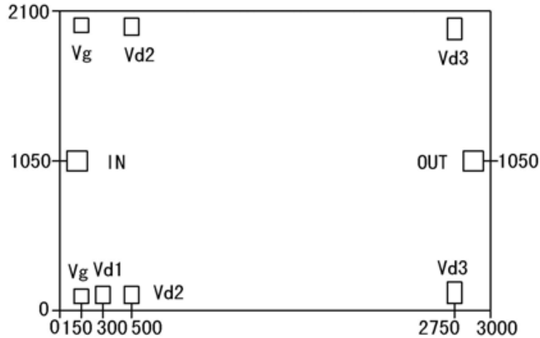
Power Gain vs. Frequency



VSWR in vs. Frequency

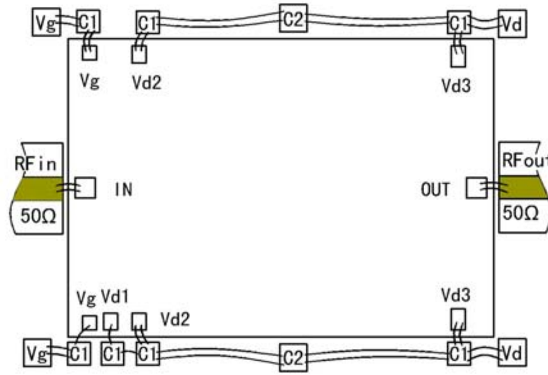


Dimension and outline



Note： All units are (μm), input and output dimension is 140×140μm^2, Bonding pad of Vg is 100×100μm^2， bonding pad of Vd1, Vd2 is 100×120μm^2， bonding pad of Vd3 is 100×150μm^2， dimension tolerance is ±50μm.

Assembly Chart



Note：External capacitor C1=100pF，C2=10000pF

Attention：

1) The substrate of 6H-SiC is easy to break, please handle carefully

2) The coefficient of thermal expansion of carrier shall be close to 6H-SiC, value shall be 4.2×10^{-6}/℃, the material of carrier is suggested for CuMoCu, CuMo or CuW.

3) Gold wires (diameter: 25μm) are suggested for bonding. The temperature of bonding platform shall not exceed 250℃.

4) Bonding with 80/20 Au/Sn. Temperature should be lower than 300℃ and time should be less than 30 seconds.

5) Blocking capacitors in Input/Output are already integrated, and Grounding short-circuit structure is integrated in input port.

6) When power on, put Gate Voltage first, then Drain Voltage. When power off, lower down Drain Voltage first, then Gate Voltage.

7) QF089 Package can be chosen for surface mounted selection.

Features

- Frequency：14GHz - 18GHz
- Power Gain：22dB
- Psat：39.5dBm
- P.A.E.：35%
- +28V@0.5A(static)
- Chip Size：2.30mm×1.50mm×0.10mm

DC Electrical Specification（T_A = +25℃）

Parameter	Min.	Typ.	Max.	Unit
Vd	-1.8	-1.9	-2.0	V
Vg	20	28	32	V
Id	0.3	0.5	0.6	A
Idd	-	1	1.3	A
Ig	-	0.1	1	mA
Igg	-	1.5	3	mA

Microwave Electrical Specification（T_A=+25℃，Vd=+28V，Vg=-1.9V）

Parameter	Min.	Typ.	Max.	Unit
f	14-18			GHz
Psat	39	39.5	-	dBm
Gp	22	23.0	24.0	dB
△Gp	-	-	±0.4	dB
PAE	30	35	-	%
Gain	28	30	32	dB
△Gain	-	-	±2	dB
VSWR(in)	-	2.0	2.5	-

Note： 1）All chips have been on-chip 100% DC tested, 100% RF tested

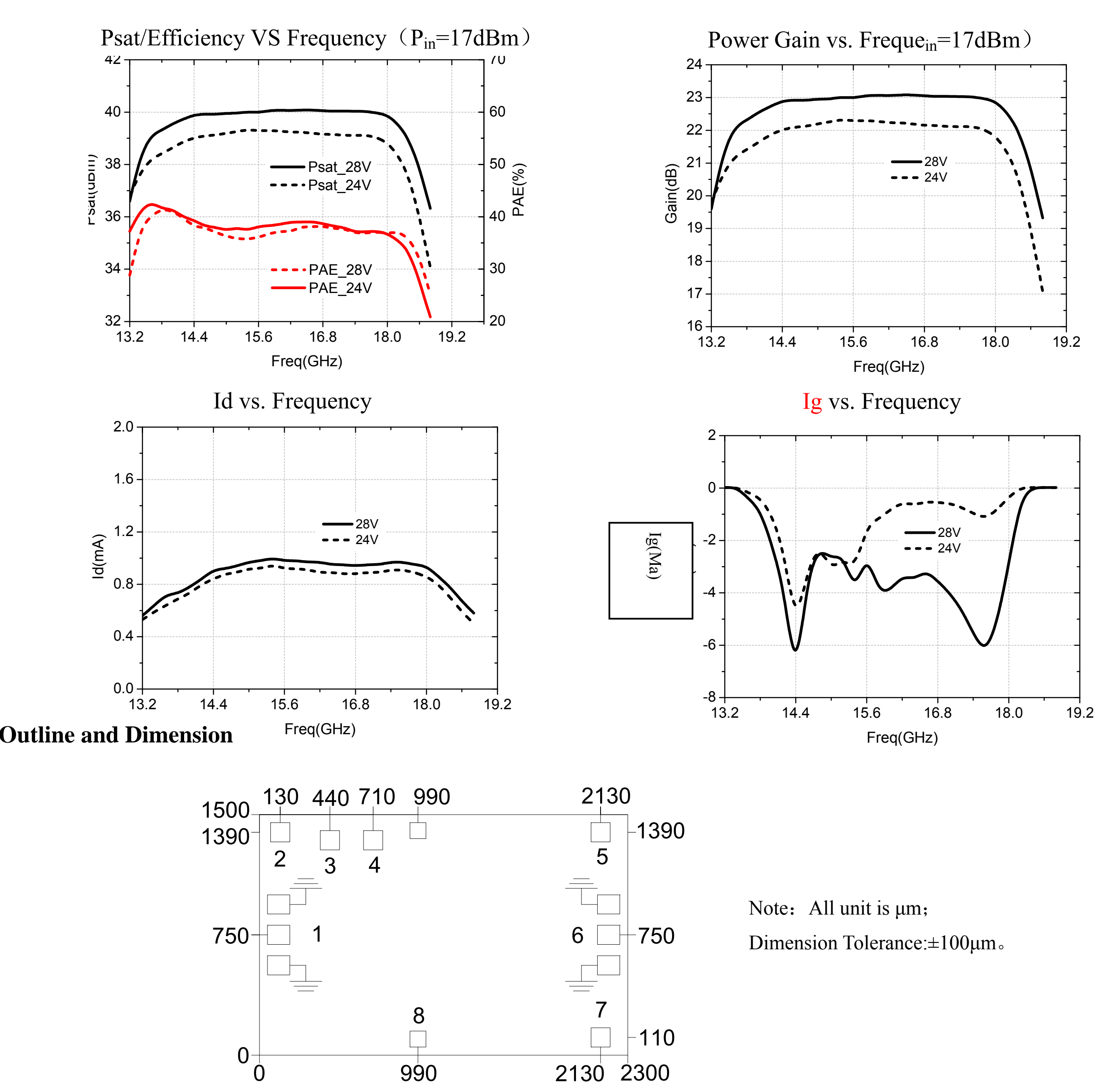
2) Test Condition : Vd=+28V，Vg=-1.9V，P_{in}=17dBm，pulse width :1ms，duty cycle :10%；

3）Recommendations resistance value for thermal simulation ：6℃/W（test condition：DC:28V/0.32A，Thermal power dissipation :9W，Ambient temperature :100℃）。

Limited Rating Values

Vds	+40V
Vgs	-6V
Max Pin（CW）	+29dBm
Max operating channel temperature	+200℃
Storage temperature	-65℃～+150℃
Load impedance mismatch (anti burn)	6：1

Typical Testing Curves（Vd=+28V，Vg=-2V）

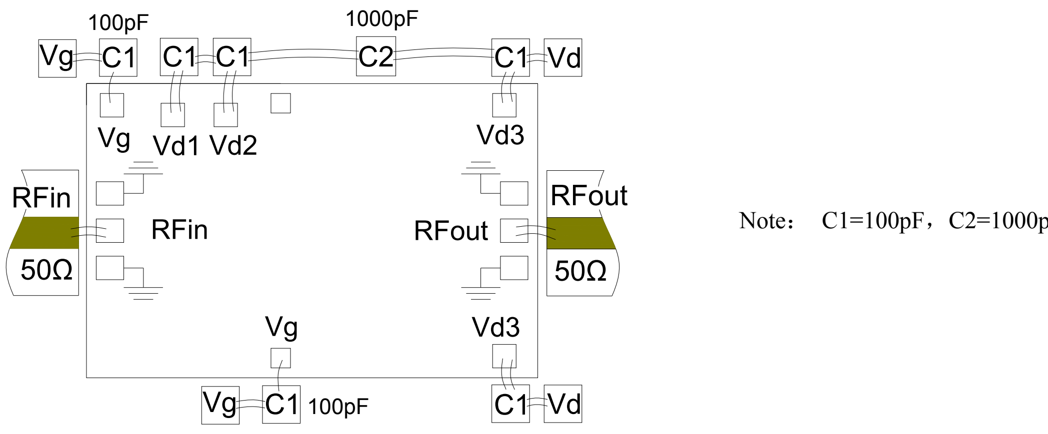


Outline and Dimension

Pad arrangement

No	Symbol	Function	Size
1	RFin	Input Pad	140×120μm^2
2	Vg	Vg bonding pad	120×120μm^2
3	Vd1	Vd bonding pad	120×120μm^2
4	Vd2	Vd bonding pad	120×120μm^2
5,7	Vd3	Vd bonding pad	120×120μm^2
6	RFout	Output Pad	140×140μm^2
8	Vg	Vg bonding pad	100×100μm^2

Assemble Diagram



Note： C1=100pF，C2=1000pF

Attention

1） Bonding with 80/20 Au/Sn. The temperature should be lower than 300℃ and time should be less than 30 seconds.
2） Blocking capacitors in Input/Output are already integrated.
3） Antistatic protection should be taken.

Features

- Frequency：4GHz～8GHz
- Power Gain：23dB
- Psat：45dBm
- P.A.E.：36%
- +28V@1.5A(static)
- Chip Size：3.55mm×4.17mm×0.10mm

Electrical Specification（TA=+25℃，Vd=+28V，Vg=-1.8V）

Parameter	Min.	Typ.	Max.	Unit
Frequency	4-8			GHz
Psat		45		dBm
Power Gain		23		dB
Small Signal Gain Flatness		±3		dB
P.A.E.	36			%
VSWRin			2.4	-
Operating Current	2.8			A

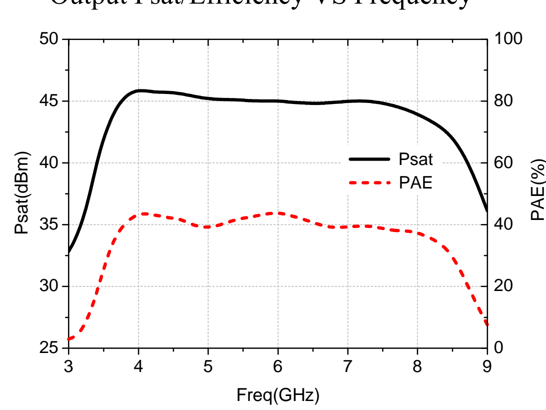
Note：1) All chips have been on-chip 100% DC and RF tested.

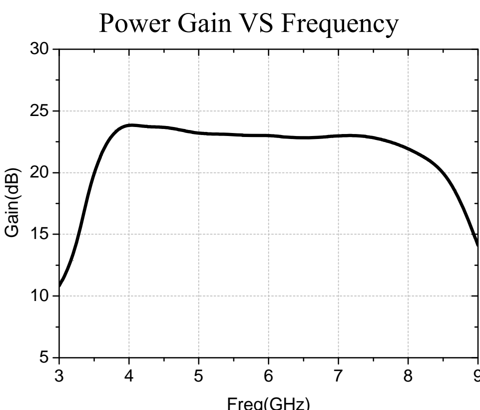
2）Test Condition：Vd=+28V，Vg=-1.8V，P_{in}=22dBm，pulse width : 100μs，duty cycle：10%.

Limited Rating Values

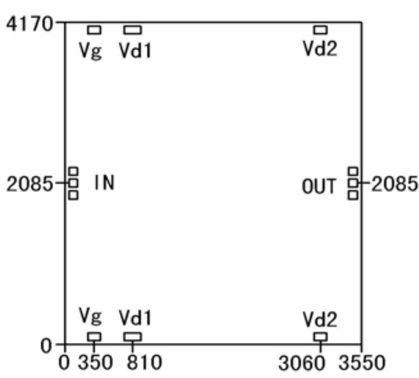
Max. Bias Vds	+32V
Min. Bias Vgs	-3V
Max. Input Power	+25dBm
Operating Temperature	-55℃～+125℃
Storage Temperature	-65℃～+150℃

Typical Testing Curves



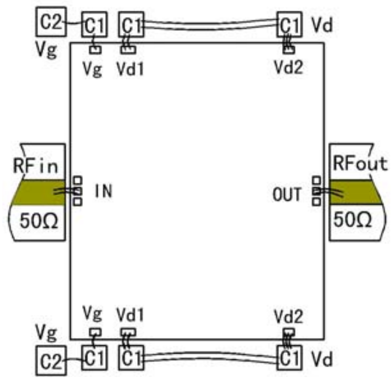


Dimensions and Outline



Note： The unit is um. Dimension of input/output pad: 100×100μm^2. Dimension of bias gate pad and second stage bias drain pad: 150×100μm^2. Dimension of first stage bias drain pad: 200×100μm^2. Dimension tolerance:±50μm.

Assembly Diagram



Note：External capacitor C1=100pF，C2=1000pF.

Attention

1) Gold bonding wires(diameter:25~30μm) are suggested to be used. Temperature of the bonding platform bottom should not exceed 250℃.
2) Blocking capacitors are already integrated for Input/Output.
3) Antistatic protection should be taken.

Features

- Frequency：2.0GHz～4.0GHz
- Power Gain：20 dB
- Psat：45dBm
- P.A.E.：40%
- +28V@2.1A(quiescent current)
- Chip Size：3.00mm×4.75mm×0.10mm

Electrical Specification (TA=+25℃，Vg=-2.0V，Vd=+28V)

Parameter	Min.	Typ.	Max.	Unit
Frequency	2.0～4.0			GHz
Psat	45			dBm
Power Gain	20			dB
Gain Flatness			±0.3	dB
P.A.E.		40		%
VSWRin			2.5	-
Operating Current			3.5	A

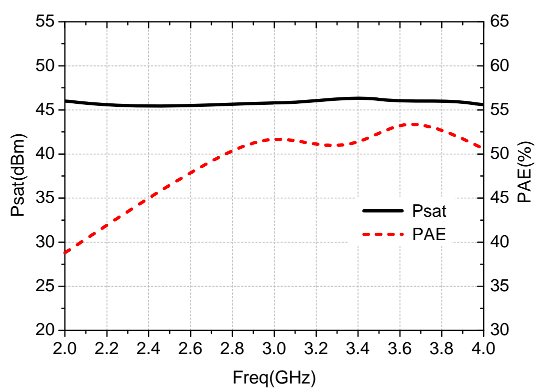
Note：1）All chips have been on-chip 100% DC and RF tested@ Vd=+28V；Vg =-2.0V，Pin=24dBm。
2) Test condition：Vd=+28V；Vg =-2.0V，Pin=24dBm.

Limited Rating Values

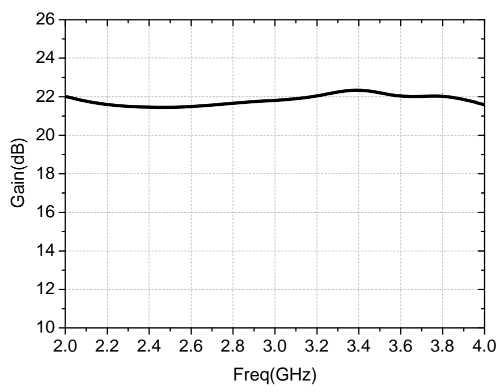
Vds	+32V
Vgs	-5V
Input CW Power	+30dBm
Channel Temperature	+175℃
Storage Temperature	-65℃～+150℃

Typical Testing Curves

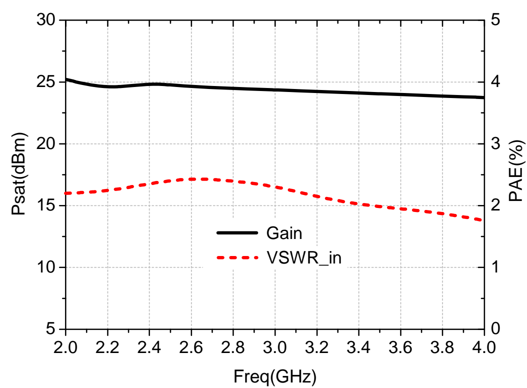
Output Psat/Efficiency VS Frequency



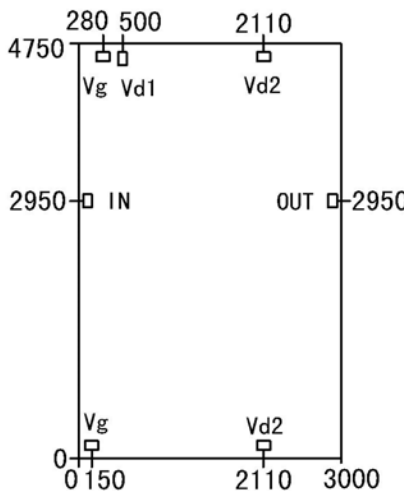
Power Gain VS Frequency



Input Voltage VSWR Ratio/Gain VS Frequency



Dimensions and Outline



Note：The unit is um.

Dimension of input/output pad：100×150μm^2.

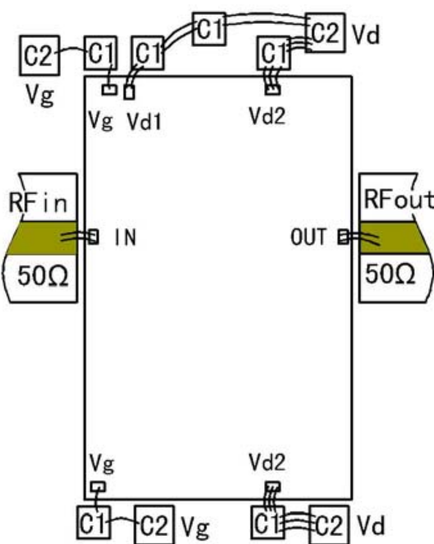
Dimension of bias pad Vg：150×100μm^2.

Dimension of bias pad Vd1：100×150μm^2.

Dimension of bias pad Vd2: 150×100μm^2.

Dimension tolerance: ±50μm.

Assembly Diagram



Note：External capacitor C1=1000pF, C2=10000pF.

Attention

1） Bonding with 80/20 Au/Sn. The temperature should be lower than 300℃ and the time should be less than 30 seconds.

2） Gold wires (diameter: 25μm～30μm) are suggested to be used. The temperature of bonding platform should not exceed 250℃

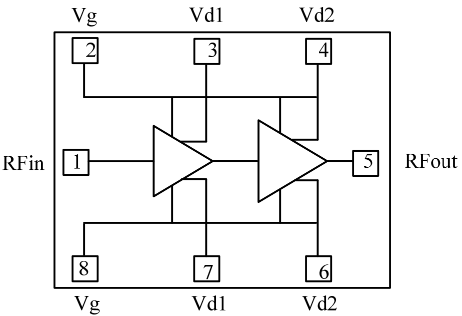
3） Blocking capacitors in Input/Output are already integrated.

4） Antistatic protection should be taken.

Features

- Frequency：5.0GHz～6.0GHz
- Power Gain：19dB
- Saturation Output Power：46dBm
- P.A.E：40%
- +28V@2.0A(Quiescent)
- Dimension：3.00mm×4.20mm×0.08mm

Block Diagram



DC Testing Electrical Specification（T_A = +25℃）

Parameters	Symbol	Min.	Typical	Max	Unit
Gate Voltage	Vd	-1.8	-2	-2.2	V
Drain Voltage	Vg	20	28	32	V
Quiescent Drain Current	Id	1.5	2.0	2.5	A
Dynamic Drain Current	Idd		2.0	2.5	A
Quiescent Gate Current	Ig		0.1	1	mA
Dynamic Gate Current	Igg		1.5	3	mA

Microwave Electrical Specification（T_A = +25℃，Vd = +28V，Vg = -2V）

Parameters	Symbol	Min.	Typical	Max	Unit
Frequency	f	5.0～6.0			GHz
Saturation Power Output	Psat	46			dBm
Power Gain	Gp	19	21.0		dB
Power Gain Flatness	△Gp			±0.2	dB
Power Added Efficiency	PAE	40			%
Linear Gain	Gain	32	34	35	dB
Linear Gain Flatness	△Gain			±0.5	dB
VSWRin	VSWR(in)		2.0	2.5	-
Second Harmonics				-30	dBc

Note：1）All chips have been 100% DC tested and 100% RF tested；

2）The condition for curve testing：Vd=+28V，Vg=-2V，P_{in}=26dBm，bandwidth 1ms，duty cycle 30%；

Linear parameter input power：P_{in}=-10dBm；

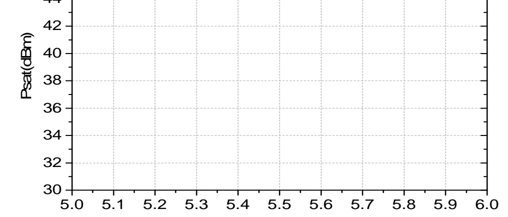
3）Thermal Resistant is suggested when thermal simulation 1.2℃/W。

Limited Rating Values

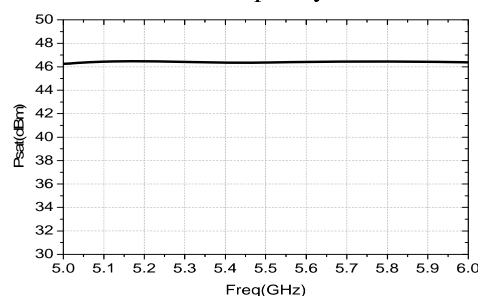
Parameters	Symbol	Values
Max V_{DS}	Vd	+40V
Max V_{GS}	Vg	-6V
Max Input Power（CW）	P_p	+30dBm
Storage Temperature	T_{STG}	-65℃～+150℃
Max Operation Channel Temperature	T_{op}	+200℃
Impedance Mismatch	Z_0	6：1

Typical Testing Curves（Vd=+28V，Vg=-2V）

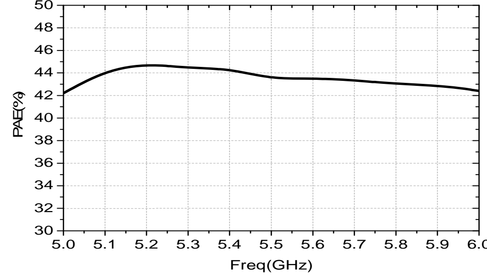
Saturation Pout vs. Frequency（P_{in}=27 dBm）



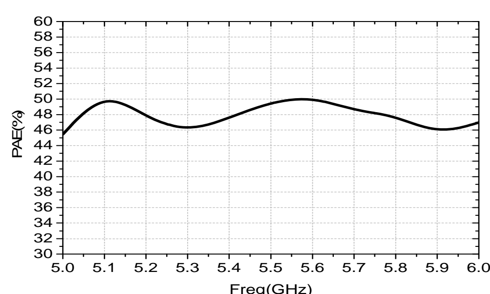
Saturation Pout vs. Frequency（P_{in}=28 dBm,Vd=28V(5ms,25%))



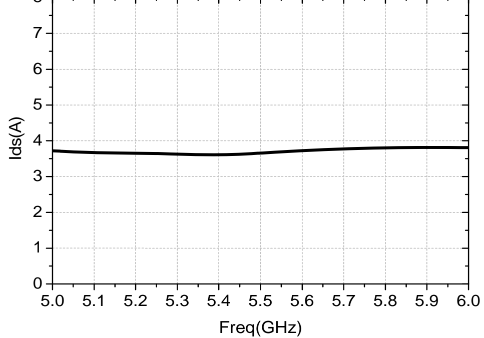
P.A.E vs. Frequency（P_{in}=27dBm）



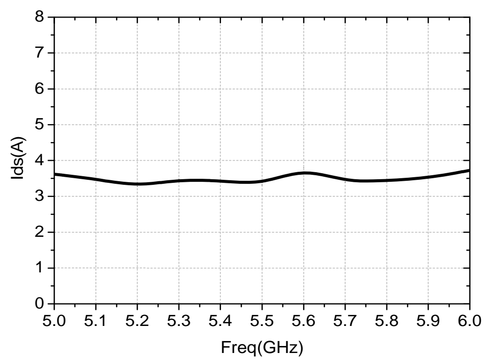
P.A.E vs. Frequency（P_{in}=28 dBm,Vd=28V(5ms,25%)）



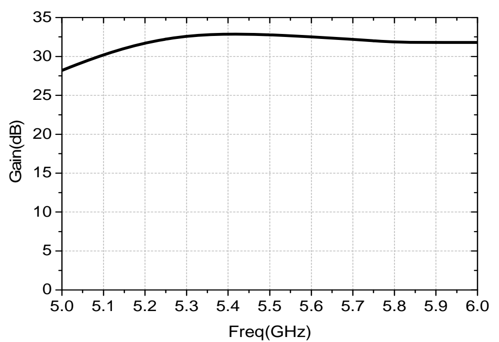
Dynamic Drain Current vs. Current



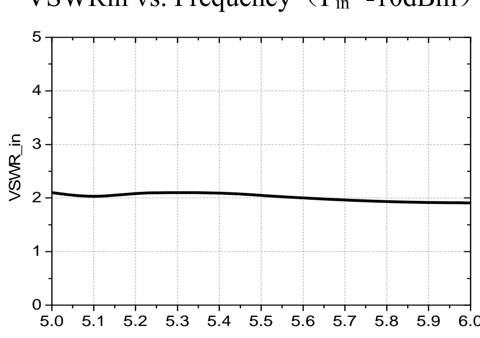
Dynamic Drain Current vs. Frequency（P_{in}=28 dBm,Vd=28V(5ms,25%)）



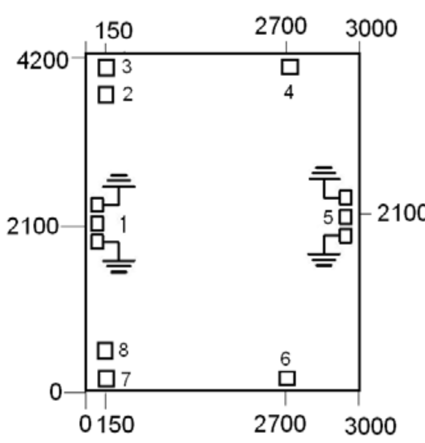
Small Signal Gain vs. Frequency（P_{in}=-10dBm）



VSWRin vs. Frequency（P_{in}=-10dBm）



Dimension and Outline



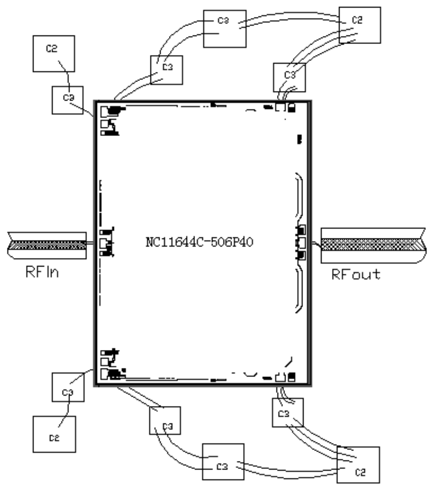
Pad Definition

Number	Symbol	Function	Dimension
1	RFin	Input Pad	100×200μm^2
2，8	Vg	Gate Bonding Pad	90×120μm^2
3，7	Vd1	Drain Bonding Pad	100×150μm^2
4，6	Vd2	Drain Bonding Pad	180×180μm^2
5	RFout	Output Pad	100×180μm^2

Note：all units are μm；

Dimension outline tolerance±100μm

Assembly Chart



Note：1）External capacitor value C3=1000pF，C2=10000pF，single layer ceramic capacitor is suggested

Attention：

1) The substrate of 6H-SiC is easy to break, please handle carefully

2) The coefficient of thermal expansion of carrier shall be close to 6H-SiC, value shall be 4.2×10^{-6}/℃, the material of carrier is suggested for CuMoCu, CuMo or CuW.

3) Gold wires (diameter: 25μm) are suggested for bonding. The temperature of bonding platform shall not exceed 250℃.

4) Bonding with 80/20 Au/Sn. Temperature should be lower than 300℃ and time should be less than 30 seconds.

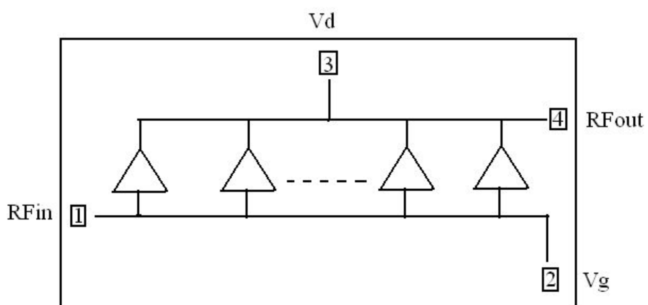
5) Blocking capacitors in Input/Output are already integrated, and Grounding short-circuit structure is integrated in input port.

6) When power on, put Gate Voltage first, then Drain Voltage. When power off, lower down Drain Voltage first, then Gate Voltage.

Features

- Frequency：2GHz～18GHz
- Power Gain：6dB
- Saturation Power Output：33dBm
- P.A.E：10%
- +28V@0.5A(Quiescent)
- Dimension：2.80mm×2.50mm×0.10mm
- 0.25μm HEMT Processing

Block Diagram



DC Electrical Specification（T_A = +25℃）

Parameters	Symbol	Min	Typical	Max	Unit
Gate Operating Voltage	Vd		-1.6	-1.8	V
Drain Operating Voltage	Vg		28	32	V
Quiescent Drain Current	Id		0.5		A
Dynamic Drain Current	Idd		0.6	0.67	A
Dynamic Gate Current	Igg		0.01	0.02	mA

Microwave Electrical Specification（T_A = +25℃，Vd = +28V，Vg = -1.6V）

Parameters	Symbol	Min	Typical	Max	Unit
Frequency	f	2～18			GHz
Saturation Power Output	Psat	33.2	34		dBm
Power Gain	Gp	6.2	7		dB
Power Gain Flatness	△Gp			±1.7	dB
P.A.E	PAE	11	15		%
Linear Gain	Gain	10	11.5		dB
Linear Gain Flatness	△Gain			±1.5	dB
Input VSWR	VSWR(in)		2.0		-
2nd Harmonics				-14	dBc

Note：1）all chips have been 100% DC and RF tested on chip；

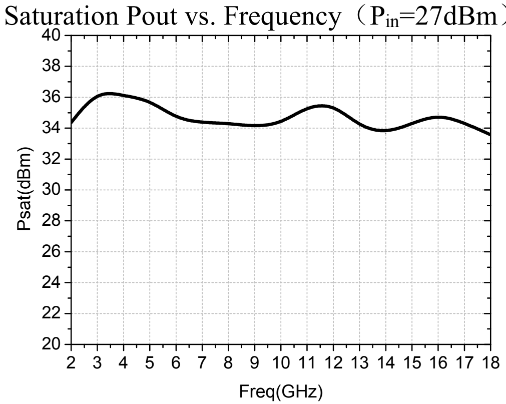
2）the testing curve testing conditions are：Vd=+28V，Vg=-1.6V，P_{in}=27dBm，CW；

Limited Rating Values

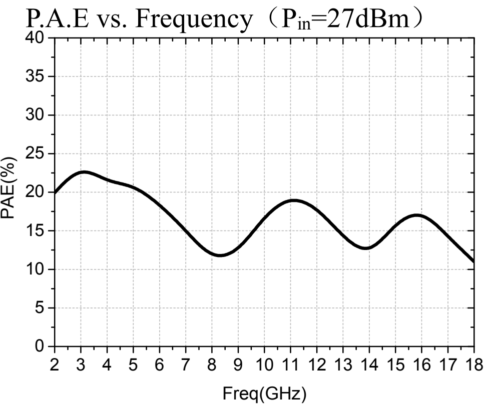
Parameters	Symbol	Limited rating values
Max Drain Source Voltage	Vd	+40V
Max Gate Source Voltage	Vg	-6V
Max Input Power（CW）	P_p	+30dBm
Storage Temperature	T_{STG}	-65℃～+150℃
Max Junction temperature	T_{op}	+200℃
Miss match of load（anti-burnt）	Z_0	6：1

Typical Testing Curves（Vd=+28V，Vg=-1.6V）

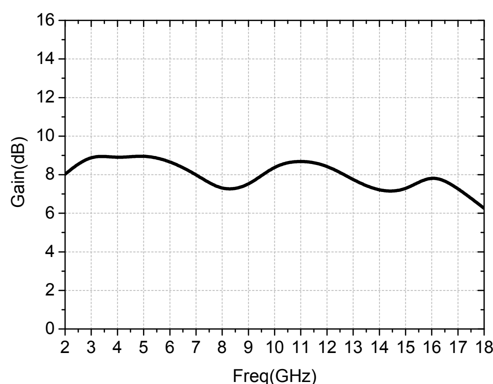
Saturation Pout vs. Frequency（P_{in}=27dBm）



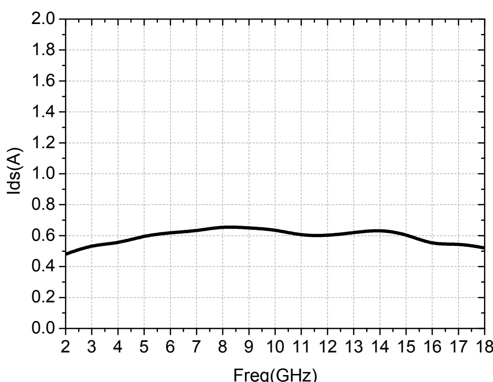
P.A.E vs. Frequency（P_{in}=27dBm）



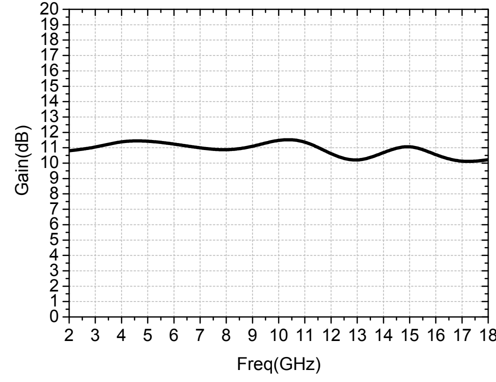
Power Gain vs. Frequency（P_{in}=27dBm）



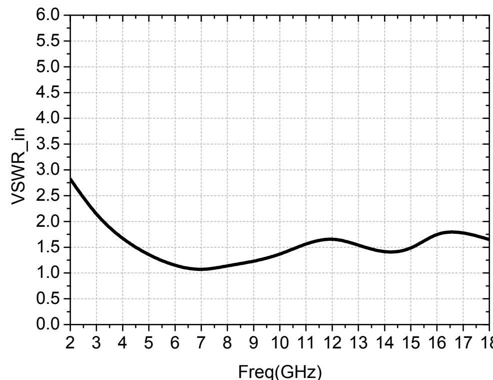
Dynamic Drain Current vs. Frequency



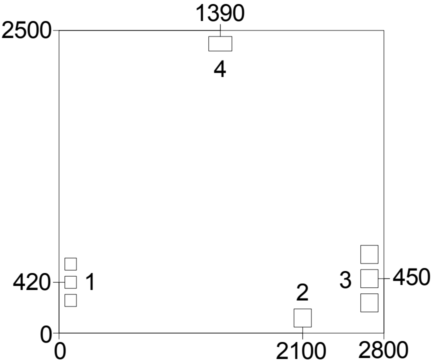
Small Signal Gain vs. Frequency（P_{in}=-10dBm）



Input VSWR vs. Frequency（P_{in}=-10dBm）



Dimension and Outline

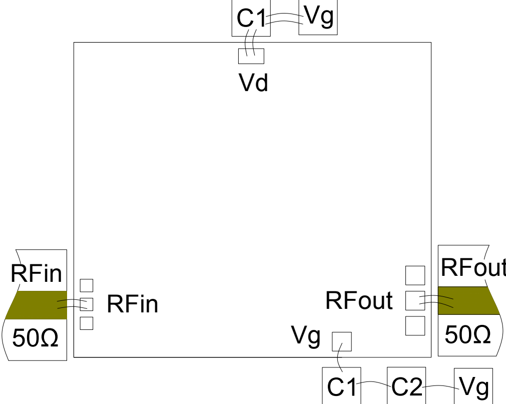


Note：all units are (μm)；
Dimension tolerance ±100μm

Pad Definition

No.	Symbol	Functions	Dimension
1	RFin	Input pad	100×100μm^2
2	Vg	Gate bonding pad	150×150μm^2
3	RFout	Output pad	150×150μm^2
4	Vd	Drain bonding pad	200×120μm^2

Assembly Chart



Note：1）external capacitor C1=100pF，C2=1000pF, single layer ceramic capacitor is recommended, and C1 shall be as close to the chip as possible, not exceeding 750μm

2）Power Circuit Micro stripe under Ku band can be soldered onto the carrier using 200μm～300μm ceramic, simplify the assembly processing. Above Ku band, it is recommended using 125μm～250μm micro stripe to solder or paste onto the carrier in order to decrease transmission loss. Input and output bonding wire length shall be within 350μm±150μm.

Attention:

1) The substrate of 6H-SiC is easy to break, please handle carefully

2) The coefficient of thermal expansion of carrier shall be close to 6H-SiC, value shall be 4.2×10^{-6}/℃, the material of carrier is suggested for CuMoCu, CuMo or CuW.

3) Gold wires (diameter: 25μm-30μm) are suggested for bonding. The temperature of bonding platform shall not exceed 250℃.

4) Bonding with 80/20 Au/Sn. Temperature should be lower than 300℃ and time should be less than 30 seconds.

5) Blocking capacitors in Input/Output are already integrated, and Grounding short-circuit structure is integrated in input port.

6) When power on, put Gate Voltage first, then Drain Voltage. When power off, lower down Drain Voltage first, then Gate Voltage.

7) QF087 Package can be chosen for surface mounted selection.

Features

- Frequency：8GHz - 12GHz
- Power Gain：24dB
- Psat：44dBm
- P.A.E.：40%
- +28V@0.8A(static)
- Dimension ：3.1mm×2.15mm×0.10mm

DC Electrical Specification（T_A = +25℃）

Parameter	Min.	Typ.	Max.	Unit
Vg	-2.8	-1.9	-1.8	V
Vd	20	28	32	V
Static drain current	0.5	0.8	1.0	A
Dynamic drain curent	-	2	2.5	A
Static gate current	-	0.1	1	mA
Dynamic gate current	-	3	5	mA

Microwave Electrical Specification（T_A=+25℃，Vd=+28V，Vg=-2V）

Parameter	Min.	Typ.	Max.	Unit
Psat	43.8	44.3	-	dBm
Power Gain	23.0	24.0	25.0	dB
Power gain flatness	-	-	±0.5	dB
P.A.E.	40	42	-	%
Liner gain	28	30	32	dB
Liner gain flatness	-	-	±2	dB
VSWRin	-	2.0	2.5	-

Note：1）All chips have been on-chip 100% DC tested.，100% RF tested；

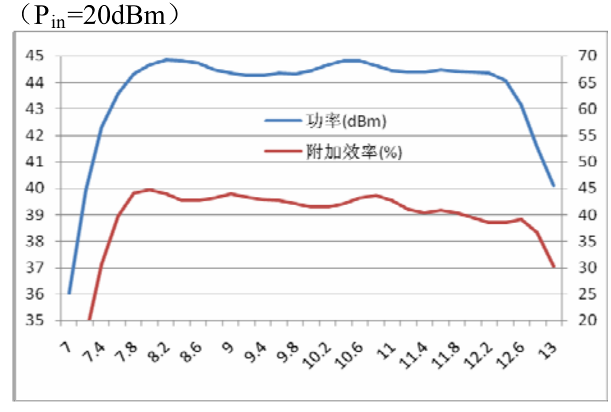
2) Test Condition：Vd=+28V，Vg=-2V，P_{in}=20dBm，pulse width 2ms，duty cycle 30%；

Limited Rating Values

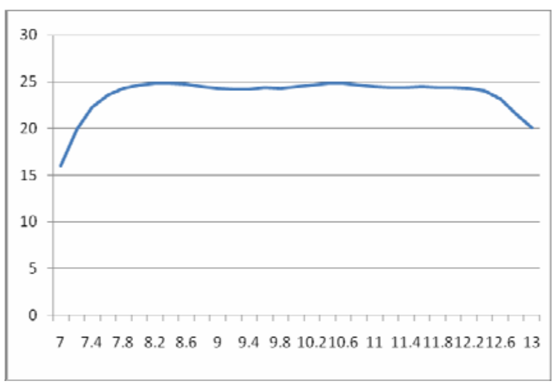
Max VDS	+40V
Min VGS	-6V
Max. Input Power（CW）	+32dBm
Max operating channel tempeature	+200℃
Storage temperature	-65℃～+150℃
Load impedance mismatch (anti burn)	6：1

Typical Testing Curves（Vd=+28V，Vg=-2V）

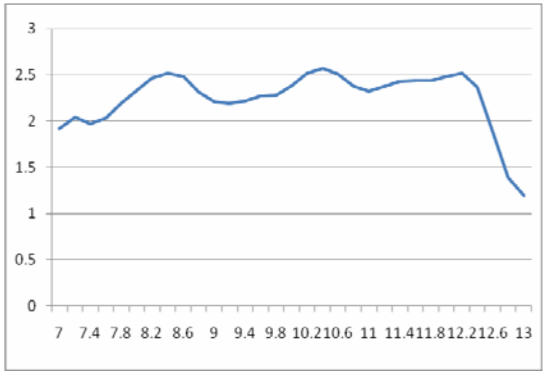
Output Psat/Efficiency VS Frequency（P_{in}=20dBm）



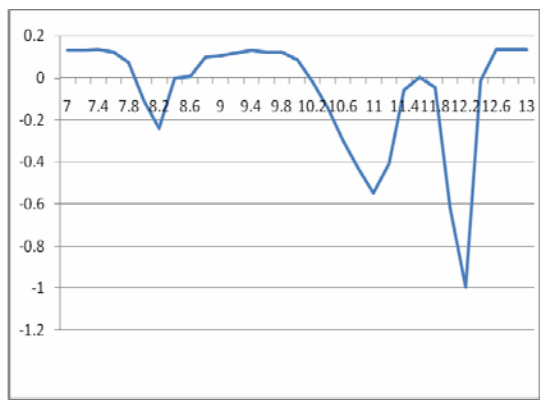
Power Gain VS Frequency（P_{in}=20dBm）



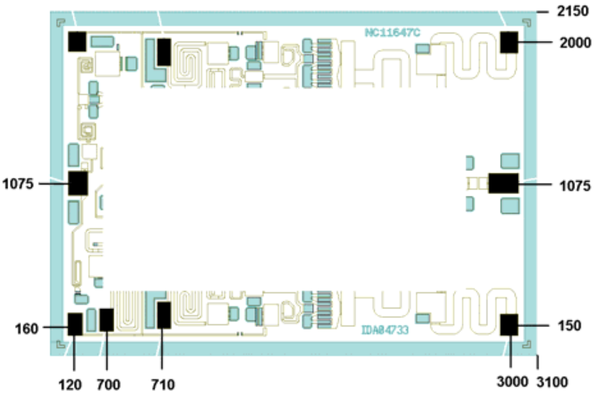
Dynamic drain current vs. Frequency



Dynamic gate current vs. Frequency



Dimensions and Outline



Note ： All the unit is μm；

Input and output pad dimension is 150×150μm^2；

Bonding pad dimension Vd1 is 120×120μm^2；

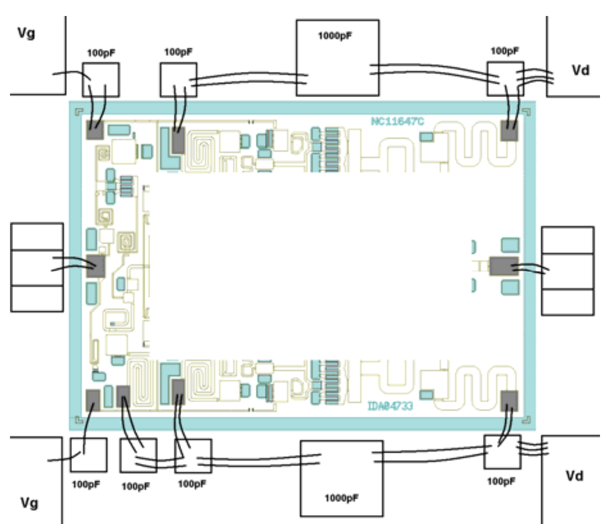
Bonding pad dimension Vd2 is 120×120μm^2；

Bonding pad dimension Vd2 is 150×150μm^2；

Bonding pad dimension Vgis140×140μm^2；

Dimension tolerance is ±100μm。

Assembly Diagram



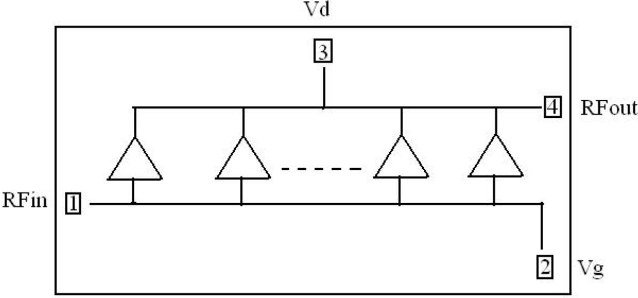
Attention

1) Bonding with 80/20 Au/Sn. The temperature should be lower than 300℃ and time should be less than 30 seconds.
2) Blocking capacitors in Input/Output are already integrated.
3) Antistatic protection should be taken.

Features

- Frequency：2GHz～18GHz
- Power Gain：6dB
- Saturation Power output：39dBm
- P.A.E：20%
- +28V@0.88A(Quiescent)
- Dimension：4.85mm×2.50mm×0.10mm
- 0.25μm HEMT Processing

Block Diagram



DC Electrical Specification（T_A = +25℃）

Parameters	Symbol	Min	Typical	Max	Unit
Gate Operating Voltage	Vd		-1.6	-1.8	V
Drain Operating Voltage	Vg		28	32	V
Quiescent Drain Current	Id		0.88	0.94	A
Dynamic Drain Current	Idd		1.2	1.35	A
Dynamic Gate Current	Igg		0.1	8	mA

Microwave Electrical Specification（T_A = +25℃，Vd = +28V，Vg = -1.6V）

Parameters	Symbol	Min	Typical	Max	Unit
Frequency	f	2～18			GHz
Saturation Power Output	Psat	39.6	40		dBm
Power Gain	Gp	6.6	7		dB
Power Gain Flatness	△Gp			±1	dB
P.A.E	PAE	20			%
Linear Gain	Gain		12		dB
Linear Gain Flatness	△Gain			±2	dB
Input VSWR	VSWR(in)		2.0		-

Note：1）all chips have been 100% DC and RF tested on chip；

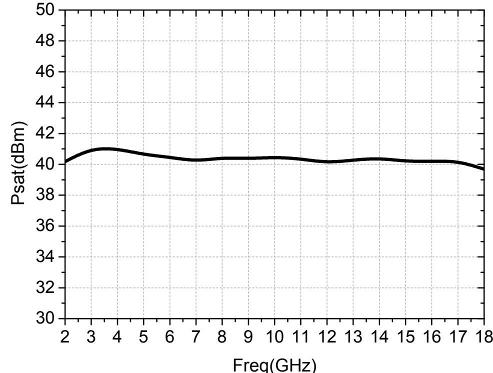
2）the testing curve testing conditions are：Vd=+28V，Vg=-1.6V，P_{in}=33 dBm，CW；

Limited Rating Values

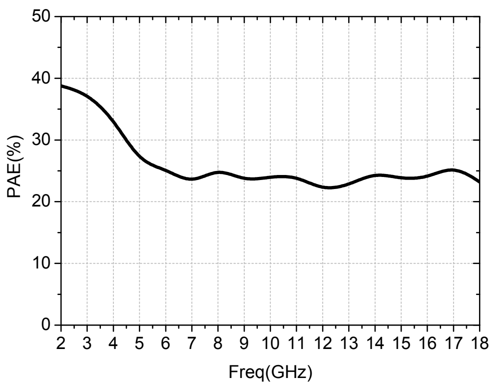
Parameters	Symbol	Limited rating values
Max Drain Source Voltage	Vd	+40V
Max Gate Source Voltage	Vg	-6V
Max Input Power（CW）	P_p	+36dBm
Storage Temperature	T_{STG}	-65℃～+150℃
Max Junction temperature	T_{op}	+200℃
Miss match of load（anti-burnt）	Z_0	6：1

Typical Testing Curves（Vd=+28V，Vg=-1.6V）

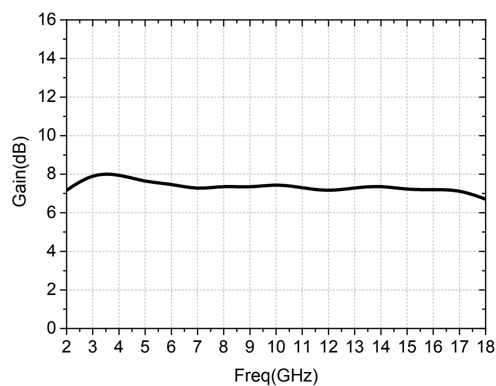
Saturation Pout vs. Frequency（P_{in}=33dBm）



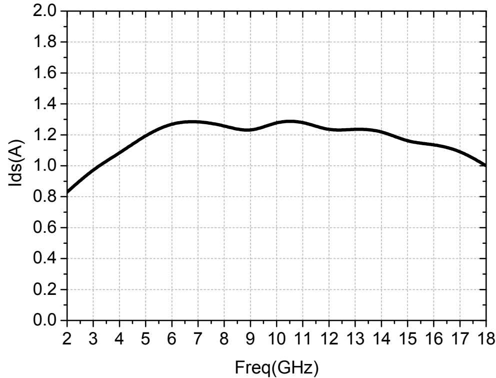
P.A.E vs. Frequency（P_{in}=33dBm）



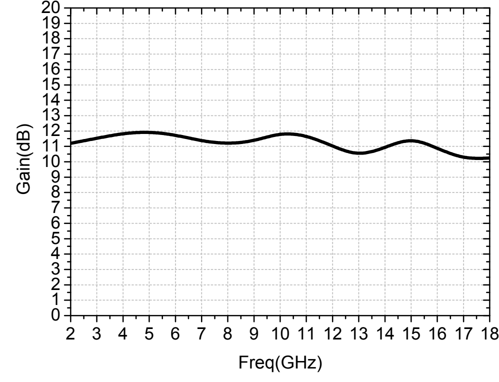
Power Gain vs. Frequency（P_{in}=33dBm）



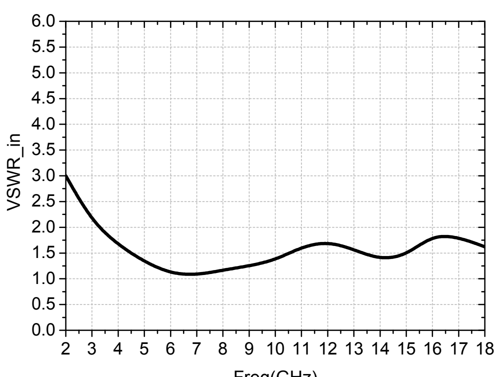
Dynamic Drain Current vs. Frequency



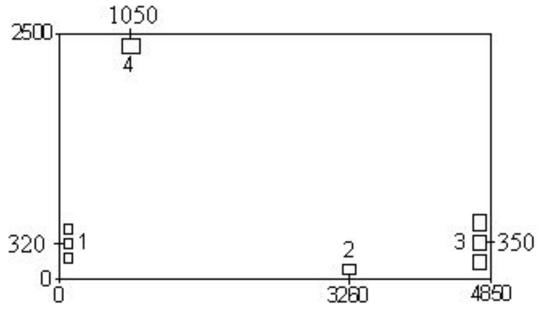
Small Signal Gain vs. Frequency（P_{in}=-10dBm）



Input VSWR vs. Frequency（P_{in}=-10dBm）



Dimension and Outline

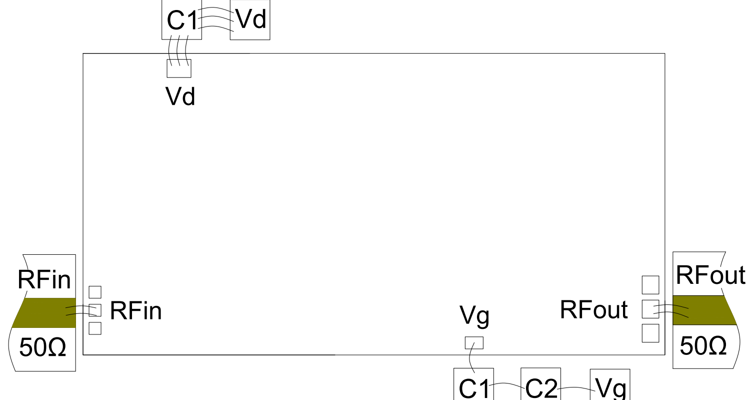


Note：all units are (μm)；
Dimension tolerance ±100μm

Pad Definition

No.	Symbol	Functions	Dimension
1	RFin	Input pad	100×100μm^2
2	Vg	Gate bonding pad	150×100μm^2
3	RFout	Output pad	140×150μm^2
4	Vd	Drain bonding pad	200×150μm^2

Assembly Chart



Note：1）external capacitor C1=100pF，C2=1000pF, single layer ceramic capacitor is recommended, and C1 shall be as close to the chip as possible, not exceeding 750μm

2）Power Circuit Micro stripe under Ku band can be soldered onto the carrier using 200μm～300μm ceramic, simplify the assembly processing. Above Ku band, it is recommended using 125μm～250μm micro stripe to solder or paste onto the carrier in order to decrease transmission loss. Input and output bonding wire length shall be within 350μm±150μm.

Attention：

1) The substrate of 6H-SiC is easy to break, please handle carefully

2) The coefficient of thermal expansion of carrier shall be close to 6H-SiC, value shall be 4.2×10^{-6}/℃, the material of carrier is suggested for CuMoCu, CuMo or CuW.

3) Gold wires (diameter: 25μm-30μm) are suggested for bonding. The temperature of bonding platform shall not exceed 250℃.

4) Bonding with 80/20 Au/Sn. Temperature should be lower than 300℃ and time should be less than 30 seconds.

5) Blocking capacitors in Input/Output are already integrated, and Grounding short-circuit structure is integrated in input port.

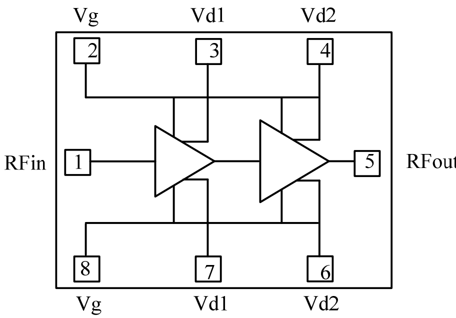
6) When power on, put Gate Voltage first, then Drain Voltage. When power off, lower down Drain Voltage first, then Gate Voltage.

7) QF087 Package can be chosen for surface mounted selection.

Features

- Frequency ： 0.9GHz～1.4GHz
- Power Gain ： 29dB
- Psat ： 45dBm
- P.A.E.： 45%
- +28V@2.0A(static)
- Chip Size ： 4.22mm×5.00mm×0.10mm

Functional Block Diagram



DC Electrical Specification（TA = +25℃）

Parameter	Symbol	Min.	Typ.	Max.	Unit
Gate Voltage	Vg	-1.8	-2	-2.2	V
Drain Voltage	Vd	20	28	32	V
Static Drain Current	Id	1.5	2.0	2.5	A
Dynamic Drain Current	Idd		2.0	2.5	A
Static Gate Current	Ig		0.1	1	mA
Dynamic Gate Current	Igg		1.5	3	mA

Microwave Electrical Specification（TA = +25℃，Vd = +28V，Vg = -2V）

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency	f	0.9～1.4			GHz
Psat	Psat	45			dBm
Power Gain	Gp	25	29.0		dB
Gain Flatness	△Gp			±0.2	dB
P.A.E.	PAE	45			%
Linear Gain	Gain	32	34	35	dB
Linear Gain Flatness	△Gain			±0.5	dB
Input VSWR	VSWR(in)		2.0	2.5	-
Second Harmonics				-30	dBc

Note：1) All chips have been on-chip 100% DC and RF tested.

2）Test condition：Vd=+28V, Vg=-2V, P_{in}=16dBm, pulse width 3ms, duty cycle 30%.

Linear Input Power：P_{in}=-10dBm；

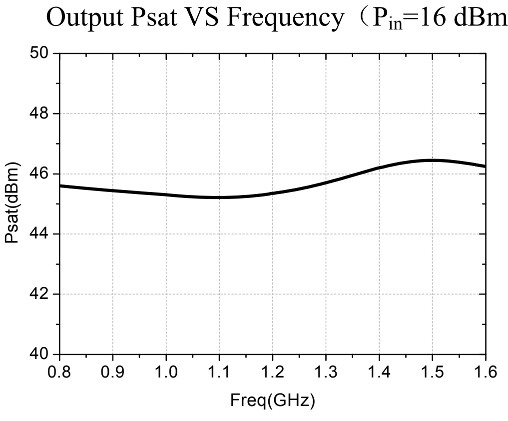
3）Suggested thermal resistance in thermal simulation: 1.2℃/W.

Limited Rating Values

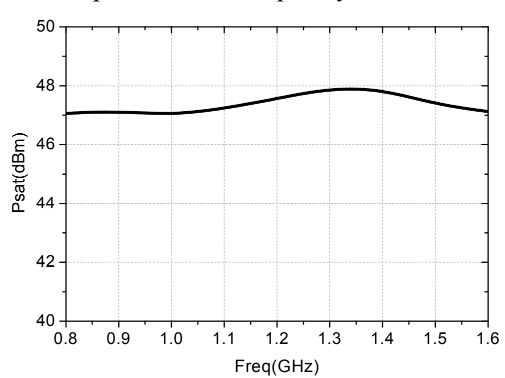
Parameter	Symbol	Value
Max. Drain Voltage	Vd	+40V
Max. Gate Voltage	Vg	-6V
Max. Input Power（CW）	P_p	+25dBm
Storage Temperature	T_{STG}	-65℃～+150℃
Max. Channel Temperature	T_{op}	+200℃
Load Impedance Mismatching（anti burn out）	Z_0	6：1

Typical Testing Curves（Vd=+28V，Vg=-2V）

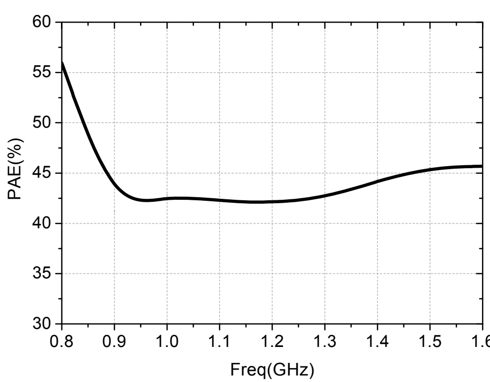
Output Psat VS Frequency（P_{in}=16 dBm）



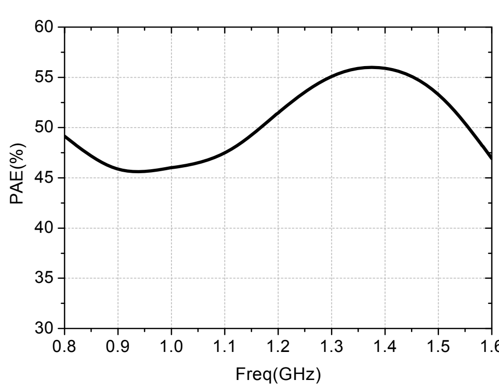
Output Psat VS Frequency（P_{in}=21 dBm）



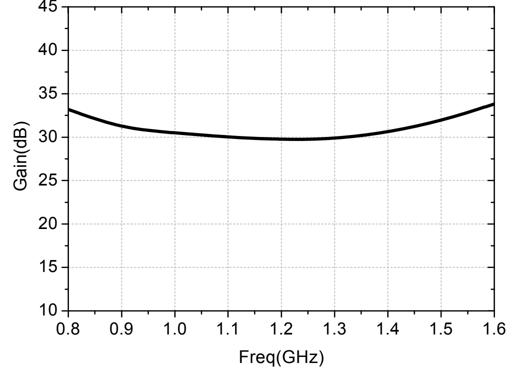
P.A.E. VS Frequency（P_{in}=16 dBm）



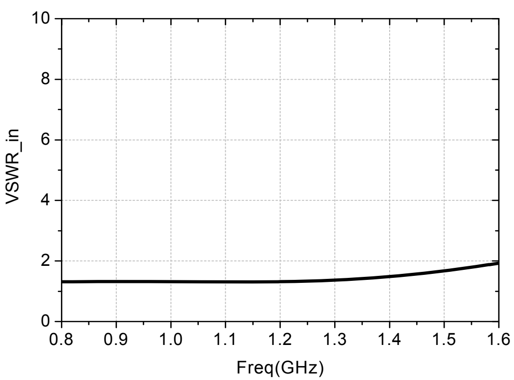
P.A.E. VS Frequency（P_{in}=21dBm）



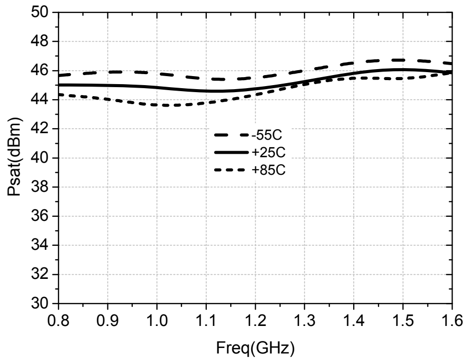
Small Signal Gain VS Frequency（P_{in}=-10dBm）



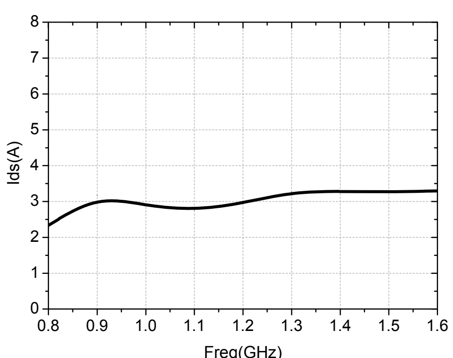
VSWRin VS Frequency（P_{in}=-10dBm）



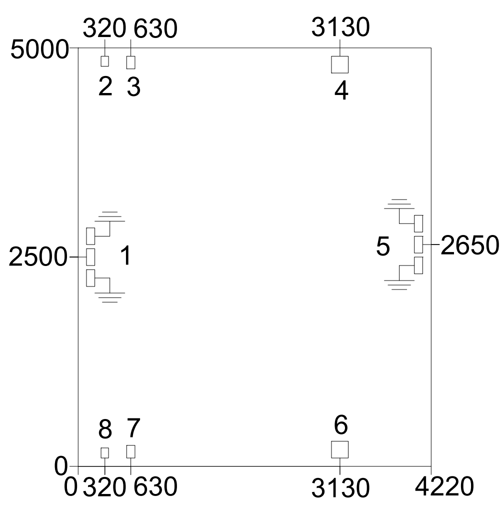
High/Low Temperature Pout VS Frequency



Dynamic Drain Current VS Frequency



Dimension and Outline



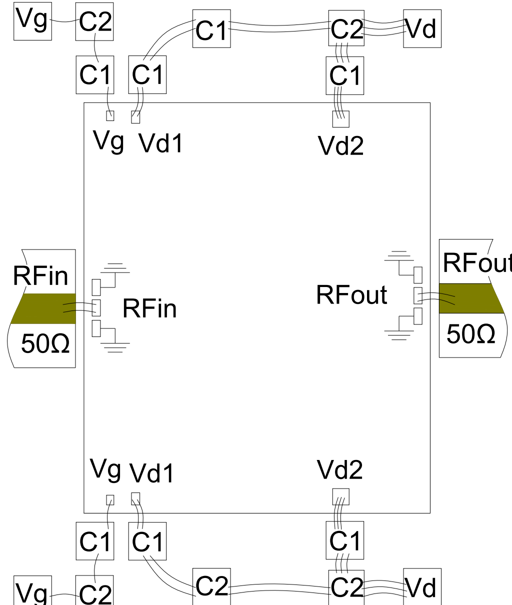
Note: The unit is um.

Dimension tolerance: ±100μm.

Pad Definition

NO.	Symbol	Function	Dimension
1	RFin	Input Pad	100×200μm^2
2，8	Vg	Gate Bonding Pad	90×120μm^2
3，7	Vd1	Drain Bonding Pad	100×150μm^2
4，6	Vd2	Drain Bonding Pad	200×200μm^2
5	RFout	Output Pad	100×200μm^2

Assembly Diagram



Note：External capacitor C1=1000pF，C2=10000pF，single layer ceramic capacitors are recommended.

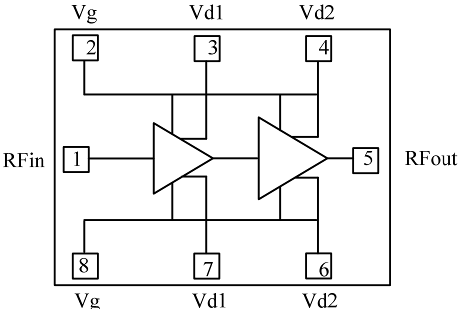
Attention

1） Bonding with 80/20 Au/Sn. The temperature should be lower than 300℃ and the time should be less than 30 seconds.
2） Gold wires (diameter: 25μm～30μm) are suggested to be used. The temperature of bonding platform should not exceed 250℃
3） Blocking capacitors in Input/Output are already integrated.
4） Antistatic protection should be taken.

Features

- Frequency ： 0.9GHz～1.2GHz
- Power Gain ： 29dB
- Psat ： 47dBm
- P.A.E.： 45%
- +28V@2.0A(static)
- Chip Size ： 4.34mm×5.00mm×0.08mm

Functional Block Diagram



DC Electrical Specification（TA = +25℃）

Parameter	Symbol	Min.	Typ.	Max.	Unit
Gate Voltage	Vg	-1.8	-2	-2.2	V
Drain Voltage	Vd	20	28	32	V
Static Drain Current	Id	1.5	2.0	2.5	A
Dynamic Drain Current	Idd		2.0	2.5	A
Static Gate Current	Ig		0.1	1	mA
Dynamic Gate Current	Igg		1.5	3	mA

Microwave Electrical Specification（TA = +25℃，Vd = +28V，Vg = -2V）

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency	f	0.9～1.2			GHz
Psat	Psat	47			dBm
Power Gain	Gp	23	26		dB
Gain Flatness	△Gp			±0.2	dB
P.A.E.	PAE	45			%
Linear Gain	Gain	32	34	35	dB
Linear Gain Flatness	△Gain			±0.5	dB
Input VSWR	VSWR(in)		2.0	2.5	-
Second Harmonics				-30	dBc

Note：1) All chips have been on-chip 100% DC and RF tested.

2）Test condition：Vd=+28V，Vg=-2V，P_{in}=16dBm，pulse width 3ms，duty cycle 30%.

Linear Input Power：P_{in}=-10dBm；

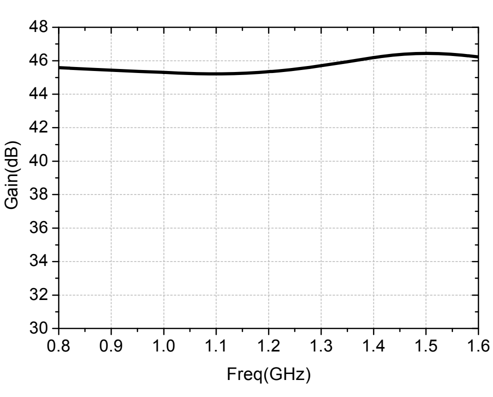
3）Suggested thermal resistance in thermal simulation : 1.2℃/W.

Limited Rating Values

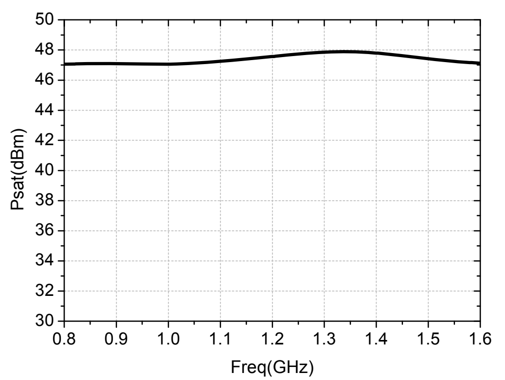
Parameter	Symbol	Value
Max. Drain Voltage	Vd	+40V
Max. Gate Voltage	Vg	-6V
Max. Input Power（CW）	P_p	+25dBm
Storage Temperature	T_{STG}	-65℃～+150℃
Max. Channel Temperature	T_{op}	+200℃
Load Impedance Mismatching（anti burn out）	Z_0	6：1

Typical Testing Curves（Vd=+28V，Vg=-2V）

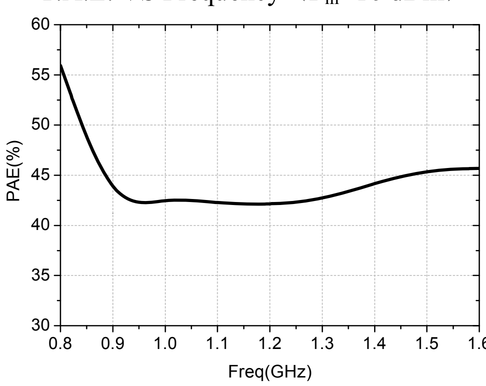
Output Psat VS Frequency（P_{in}=16 dBm）



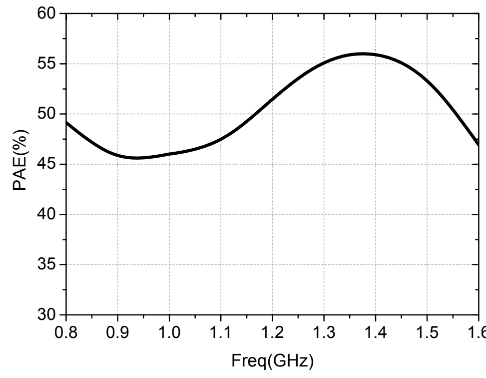
Output Psat VS Frequency（P_{in}=21 dBm）



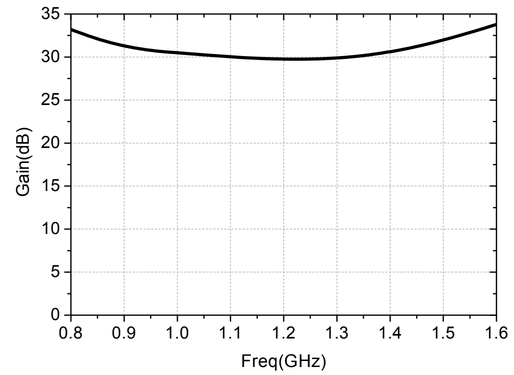
P.A.E. VS Frequency（P_{in}=16 dBm）



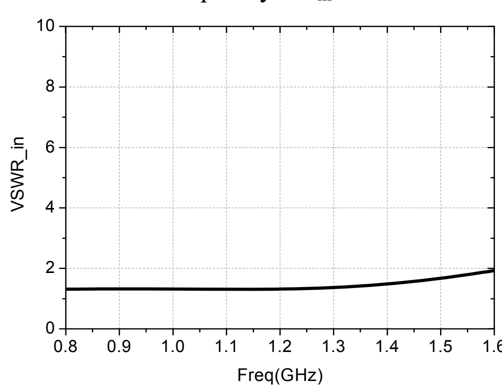
P.A.E. VS Frequency（P_{in}=21 dBm）



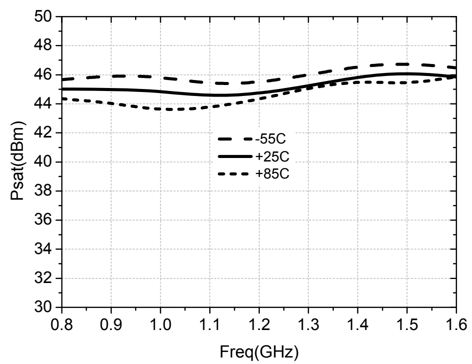
Small Signal Gain VS Frequency（P_{in}=-10dBm）



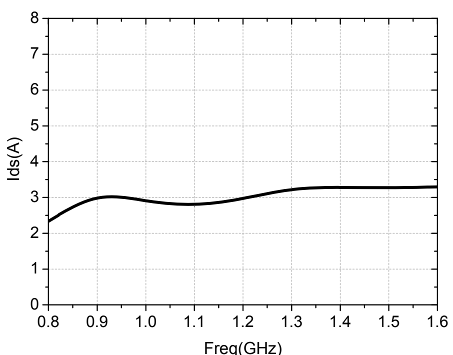
VSWRin VS Frequency（P_{in}=-10dBm）



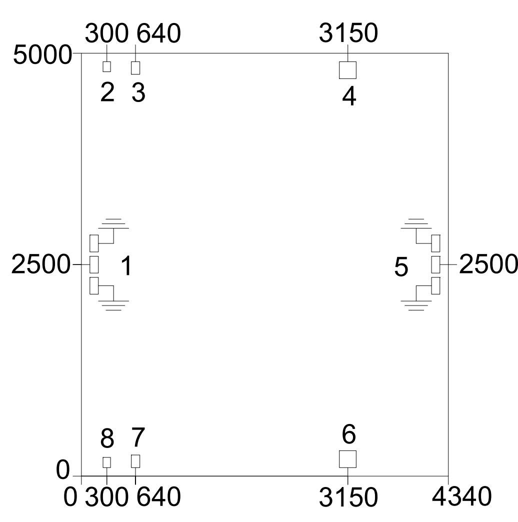
High/Low Temperature Pout VS Frequency



Dynamic Drain Current VS Frequency



Dimension and Outline



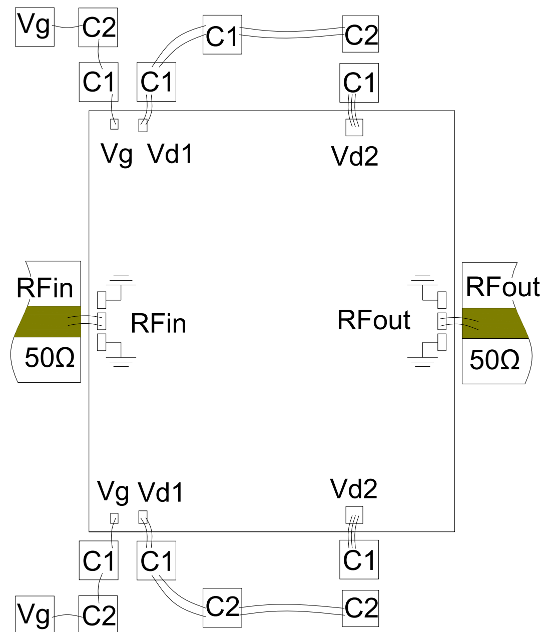
Note：The unit is um.

Dimension tolerance: ±100μm.

Pad Definition

NO.	Symbol	Function	Dimension
1	RFin	Input Pad	100×200μm^2
2，8	Vg	Gate Bonding Pad	90×120μm^2
3，7	Vd1	Drain Bonding Pad	100×150μm^2
4，6	Vd2	Drain Bonding Pad	200×200μm^2
5	RFout	Output Pad	100×200μm^2

Assembly Diagram



Note：External capacitor C1=1000pF，C2=10000pF，single layer ceramic capacitors are recommended.

Attention

1） Bonding with 80/20 Au/Sn. The temperature should be lower than 300℃ and the time should be less than 30 seconds.

2） Gold wires (diameter: 25μm～30μm) are suggested to be used. The temperature of bonding platform should not exceed 250℃

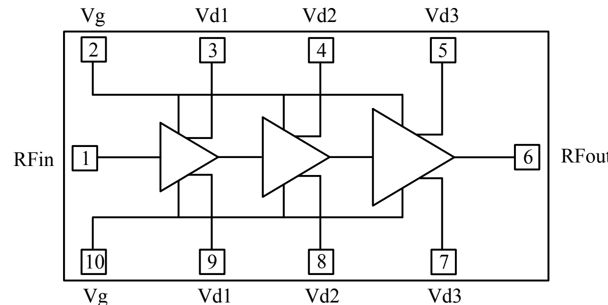
3） Blocking capacitors in Input/Output are already integrated.

4） Antistatic protection should be taken.

Features

- Frequency：6.0GHz～18.0GHz
- Power Gain：16dB
- Psat：40dBm
- P.A.E.：20%
- +28V@1400mA(static)
- Chip Size：4.10mm×3.40mm×0.08mm

Functional Block Diagram



DC Electrical Specification（TA＝+25℃）

Parameter	Symbol	Min.	Typ.	Max.	Unit
Gate Voltage	Vd		-1.8	-5	V
Drain Voltage	Vg		28	32	V
Static Drain Current	Id		1400		mA
Dynamic Drain Current	Idd		2.2	2.4	A
Dynamic Gate Current	Igg		10	25	mA

Microwave Electrical Specification（TA＝+25℃，Vd＝+28V）

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency	f	6～18			GHz
Psat	Psat	40.0	41		dBm
Power Gain	Gp	16	17		dB
Power Gain Flatness	△Gp			±0.6	dB
P.A.E.	PAE	18			%
Linear Gain	Gain		29	32	dB
Linear Gain Flatness	△Gain			±3	dB
VSWRin	VSWR(in)		2	3.5	-

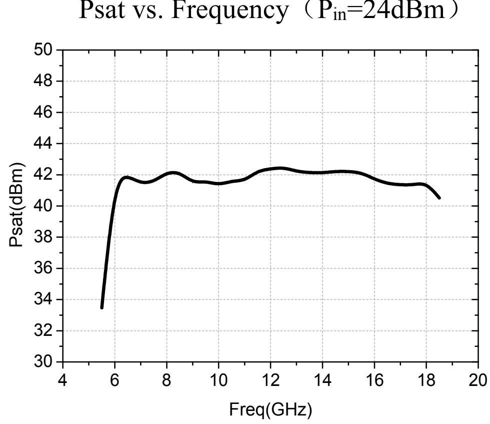
Note：1）The chip has been 100% on chip DC and RF tested.

Limited Rating Values

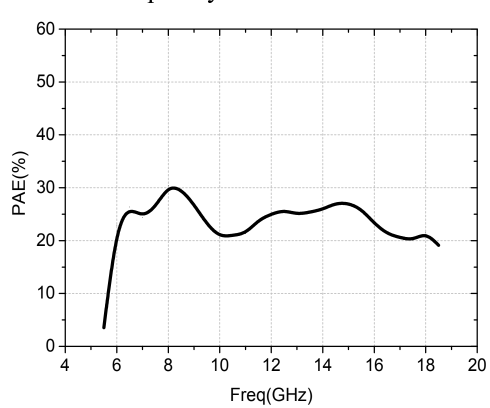
Parameter	Symbol	Value
Max. Drain Voltage	Vd	+35V
Min. Gate Voltage	Vg	-5V
Max. Input Power	Pin	+28dBm
Operating Temperature	T_{op}	-55℃～+125℃
Storage Temperature	T_{op}	-65℃～+150℃

Typical Testing Curves（Vd=+28V，Vg=-1.8V）

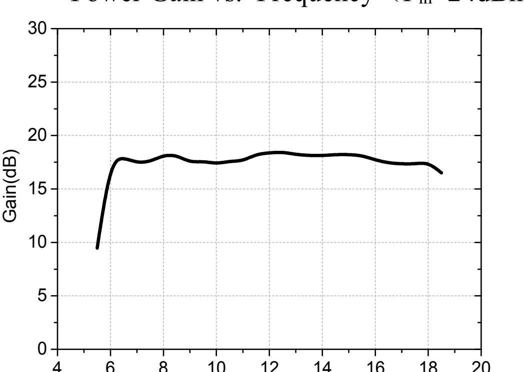
Psat vs. Frequency（P_{in}=24dBm）



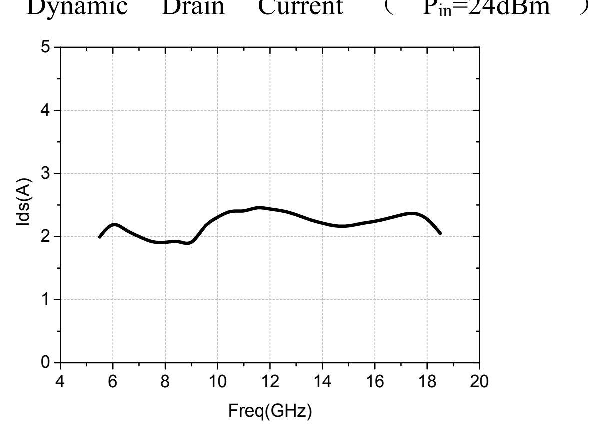
P.A.E. vs. Frequency（P_{in}=24dBm）



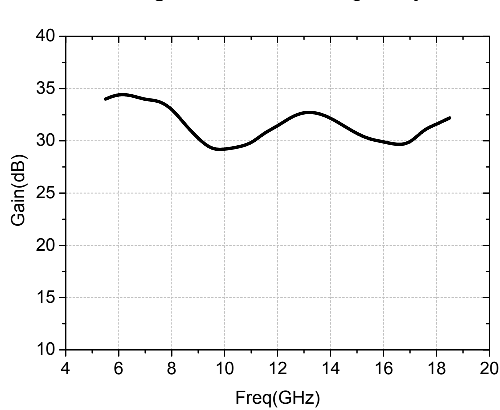
Power Gain vs. Frequency（P_{in}=24dBm）



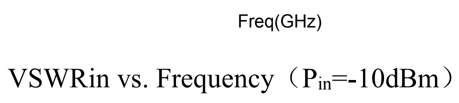
Dynamic Drain Current （ P_{in}=24dBm ）

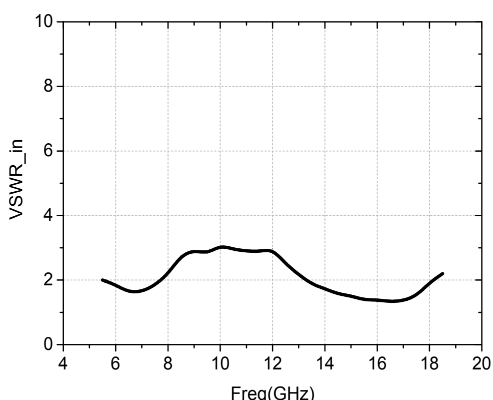


Small Signal Gain vs. Frequency（P_{in}=-10dBm）

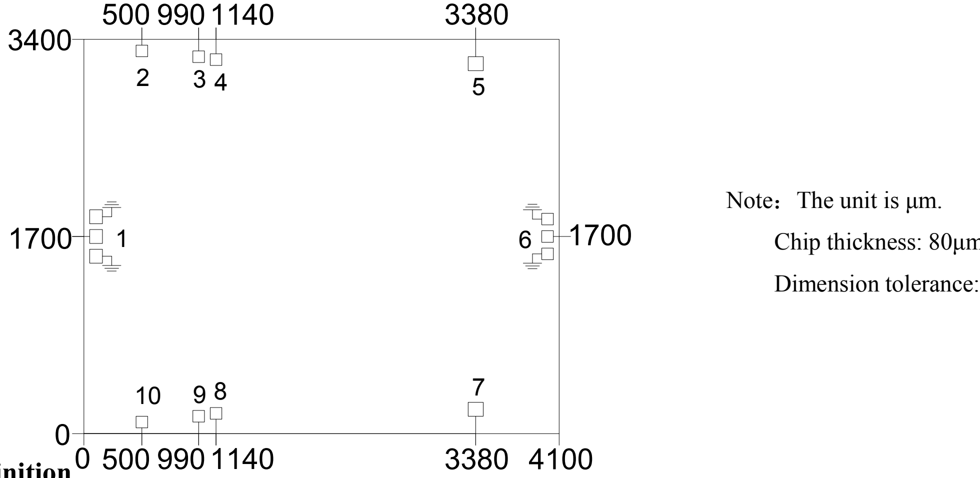


VSWRin vs. Frequency（P_{in}=-10dBm）





Dimension and Outline



Note：The unit is μm.

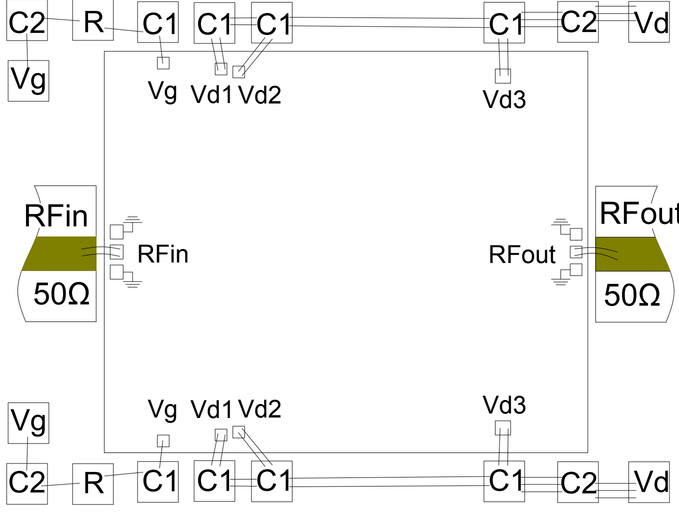
Chip thickness: 80μm.

Dimension tolerance: ±25μm.

Bonding Pad Definition

NO.	Symbol	Function	Size
1	RFin	RF signal input port, external 50 Ω system should be connected，blocking capacitor not needed.	110×120μm²
2、10	Vg	Amplifier gate pad feed port，external 100pF、1000pF filter capacitors are needed.	100×100μm²
3、9	Vd1	Amplifier drain pad feed port，external 100pF、1000pF filter capacitors are needed.	100×100μm²
4、8	Vd2	Amplifier drain pad feed port，external 100pF、1000pF filter capacitors are needed.	100×100μm²
5、7	Vd3	Amplifier drain pad feed port，external 100pF、1000pF filter capacitors are needed.	130×120μm²
6	RFout	RF signal output port, external 50 Ω system should be connected，blocking capacitor not needed.	100×100μm²

Assembly Diagram



Note：External capacitor C1=100pF，C2=1000pF. R=50Ω

Features:

- Frequency: 8GHz～12GHz
- Gain: 16dB
- Saturation Pout: 28dBm
- +28.0V@160mA
- Dimension: 1.92mm×1.33mm×0.10mm

P.A.E vs. Frequency

PAE(%)

Freq(GHz)

Electrical Specification (T_A = +25℃)

Parameter	Testing Condition V_D=28V, f: 8-12GHz	Limited Value			Unit
		Min	Typical	Max	
Saturation Pout	P_i=15dBm	-	29	-	dBm
P_{-1}	P_i=12dBm	-	28	-	dBm
Linearity Gain	P_i=-20dBm	16	17	-	dB
Linearity Gain Flatness		-0.7	-	0.7	dB
Input VSWR		-	2.0:1	-	—
Output VSWR		-	2.0:1	-	—
Operation Current		-	160	-	mA

Note: all chips have been 100% DC Tested

Power Gain vs. Frequency

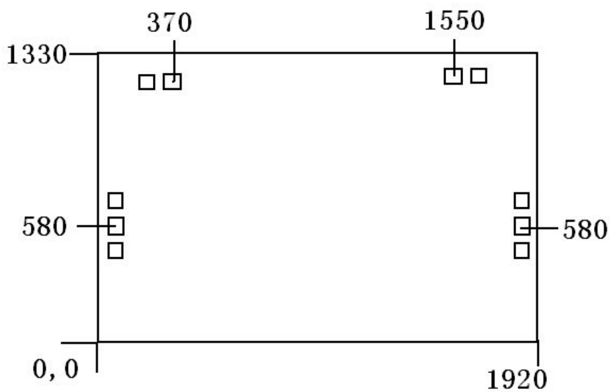
Gain(dB)

Freq(GHz)

Limited Rating Value

Symbol	Parameter	Value
V_{DS}	Positive Vgs	+32V
P_{in}	Input CW Power	+7dBm
T_{ch}	Channel Temperature	+200℃
T_{STG}	Storage Temperature	-65℃～+150℃

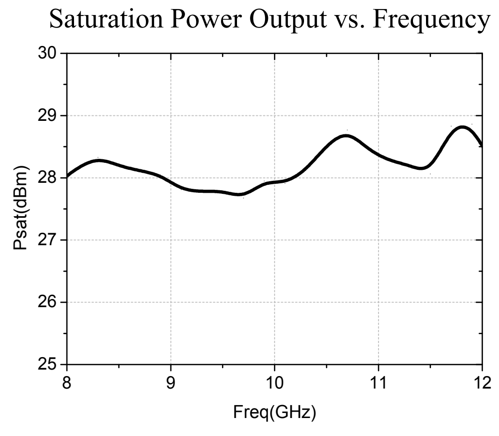
Dimension and Outline

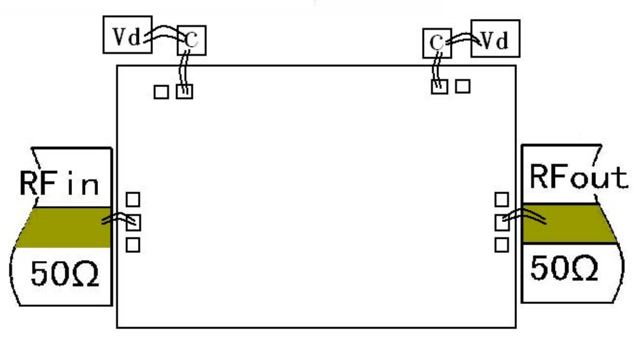


note: all units are um

Testing Curves

Saturation Power Output vs. Frequency



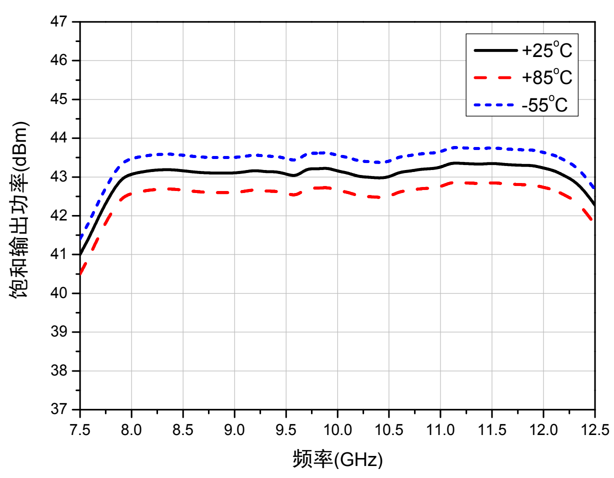


note: external capacitor value is 100pF

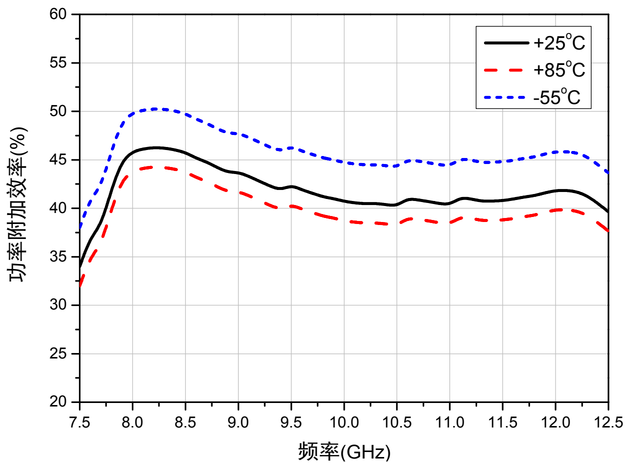
Attention

1) Diameters of 25μm～30μm shall be taken for bonding, the temperature of platform of bonding shall be less 250℃.
2) Bonding with 80/20 Au/Sn. The temperature should be lower than 300℃ and the time should be less than 30 seconds.
3) Antistatic protection should be taken.

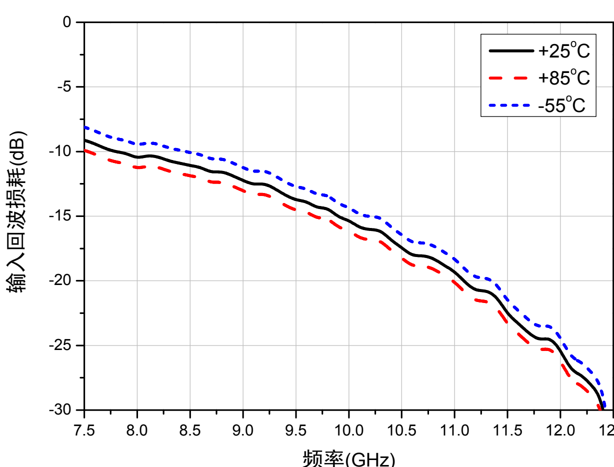
Saturation Pout VS Frequency (Pin:23dBm)



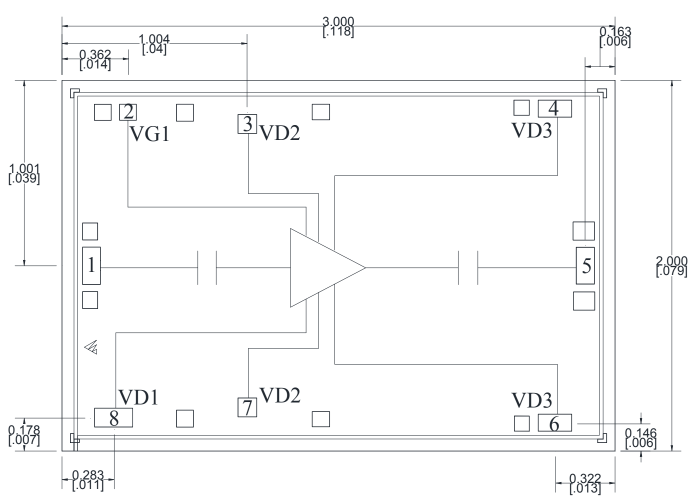
P.A.E VS Frequency (Pin:23dBm)



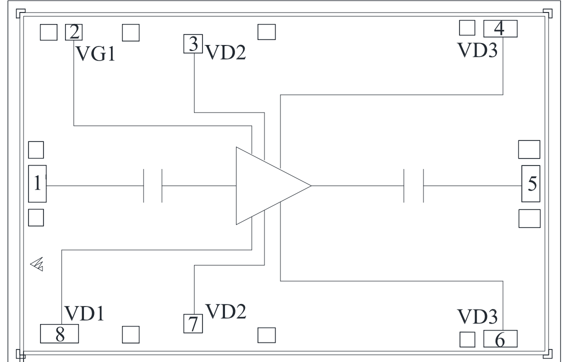
Input Return Loss VS Temperature



Dimension



Block Diagram

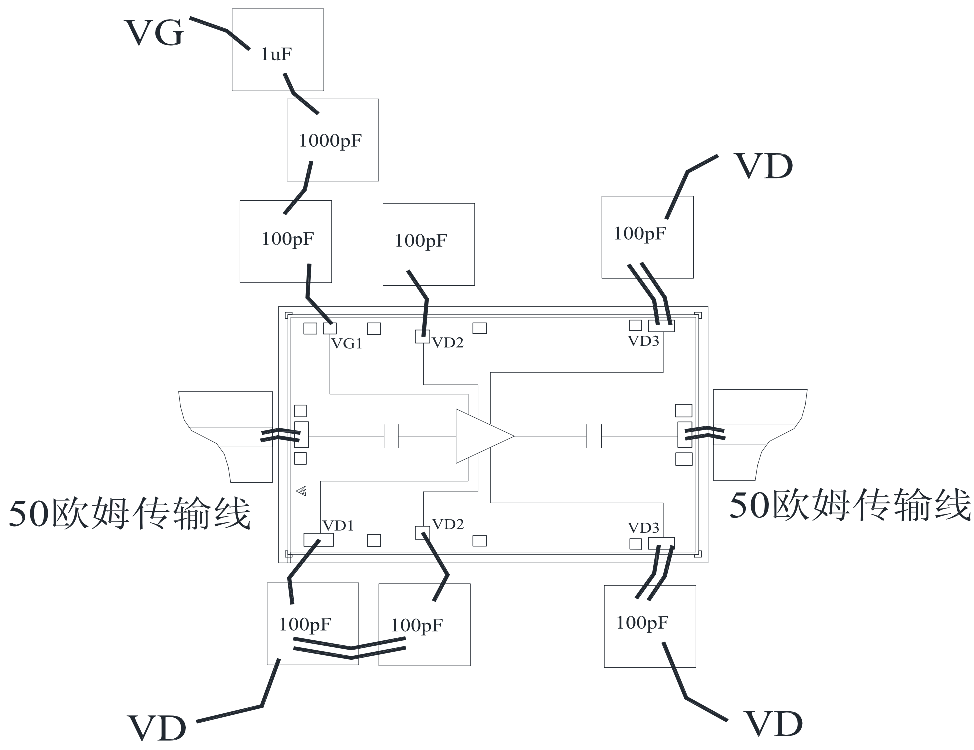


Remarks
1. Unit mm
2. Backside of MMIC gold plated and grounded
3. Bonding pad shall be gold plated
4. Pad dimension： 1、4、5、6、8： 0.20mmx0.10mm；
   2、3、7： 0.10mmx0.10mm
5. No bonding on the via hole
6. Dimension tolerance：±0.05mm

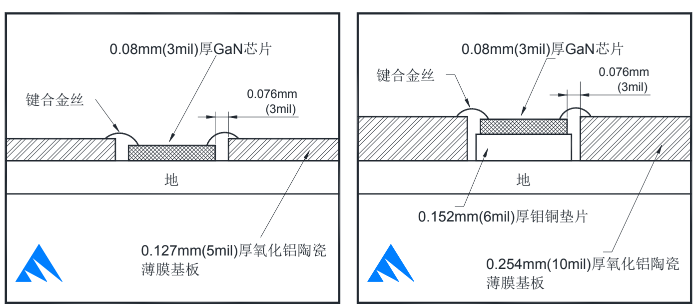
Bonding Pin Definition

Number	Function	Description	Equivalent Circuit
1	RFin	RF input, 50Ω Impedance, no blocking capacitor is needed	RFin
3、4、6、7、8	VD	External 100pF needed	Vdd
2	VG	100pF,1000pF, 1uF needed	Vgg
5	RFout	RF output, 50Ω Impedance, no blocking capacitor is needed	RFout
Back	GND		GND

1. Assembly Chart



2. Assembly Instruction



Note: Typical assembly space is 0.076~0.152 mm (3 ~ 6 mils)

METDA Semiconductor

2.7~3.5GHz 80W Power Module
Part number：HEG401E
(Updated from 3.1-3.5 GHz to 2.7-3.5GHz)

Characteristics

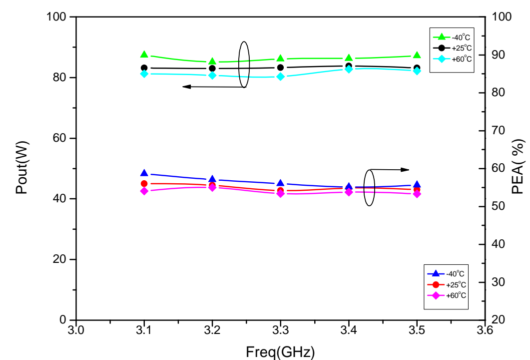
- ●Frequency range：2.7~3.5GHz
- ●50Ω impendence，easy for stages connection
- ●QF136G Package
- ●Temperature range：-55℃~+85℃

Electrical Specification

Operating condition：50Ω, Vd=28V, Vg=-5V；

（Typical Test Condition：1ms, 10% duty cycle）

Parameter	Unit	Standard	Typical
Frequency	GHz	2.7~3.5	--
Saturation Pout	dBm	≥49	49.2
Pout Flatness	dB	≤0.8	0.5
Power Gain	dB	≥9.5	10
P.A.E	--	≥50%	53%



Limited Rating Value

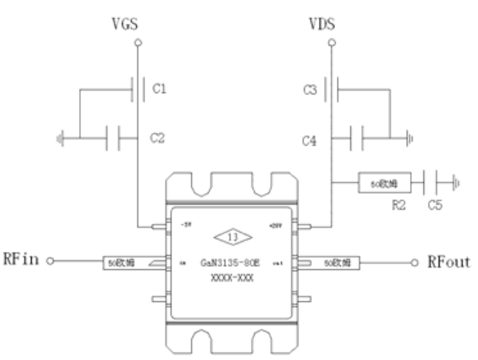
Power Supply：Vds +35V；Vgs -10V

Dissipation Power（T_A=25 ℃）：80W

Storage Temperature：-65℃~+175℃

Operation Temperature：-55 ℃~+85 ℃

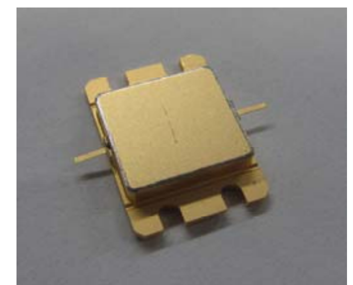
Manual



- ● QF136G Package， SMA or carrier chip can be provided upon request.
- ●Connect the circuit as left shown. Pay attention to electro-static discharging. Ensure well grounding and dissipating condition.
- ●Under the pulse operating condition, in order to realize the performance well, please adopt power filter and energy stored capacitor properly according to modulation.

2.7~3.5GHz 120W Power Module
Part number：HEG601B

Characteristics

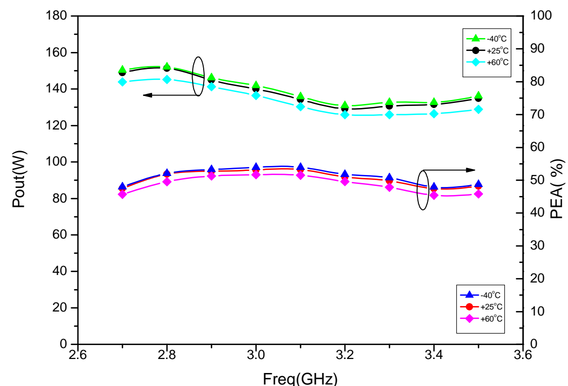


●Frequency range：2.7~3.5GHz
●50Ω impendence，easy for stages connection
●QF136H Package
●Temperature range：-55℃~+85℃

Electrical Specification

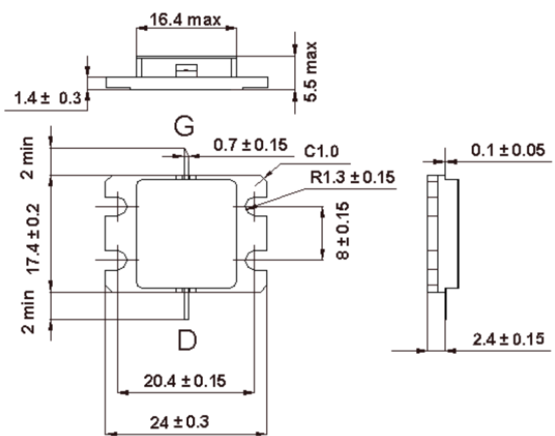
Operating condition：50Ω, Vd=28V, Vg=-5V；
（Typical Test Condition：1ms，10% duty cycle）

Parameter	Unit	Standard	Typical
Frequency	GHz	2.7~3.5	--
Saturation Pout	dBm	≥51	51.5
Pout Flatness	dB	≤0.8	0.5
Power Gain	dB	≥9.5	10
P.A.E	--	≥45%	50%

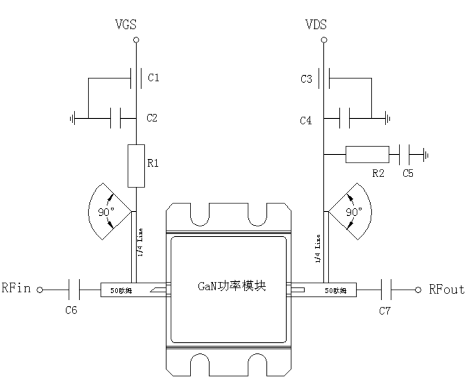


Limited Rating Value

Power Supply：Vds +35V；Vgs -10V
Dissipation Power（T_A=25 ℃）：150W
Storage Temperature：-65℃~+175℃
Operation Temperature：-55 ℃~+85 ℃



Manual



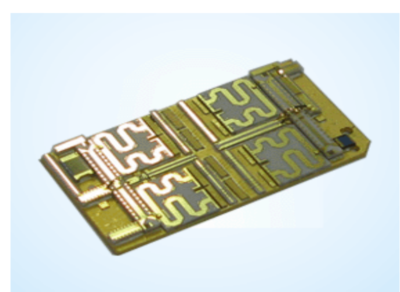
● QF136H Package，SMA or carrier chip can be provided upon request.

●Connect the circuit as left shown. Pay attention to electro-static discharging. Ensure well grounding and dissipating condition.

●Under the pulse operating condition, in order to realize the performance well, please adopt power filter and energy stored capacitor properly according to modulation.

2.7~3.5 GHz 200W Power Module HEG605A

HEG8605A is a GaN Internally Matched Module based on our own GaN device with advanced flat internally matching technology/thin film integration technology. It can cover the frequency of 2.7-3.5 GHz, can be operating in both CW and Pulse condition.



Features

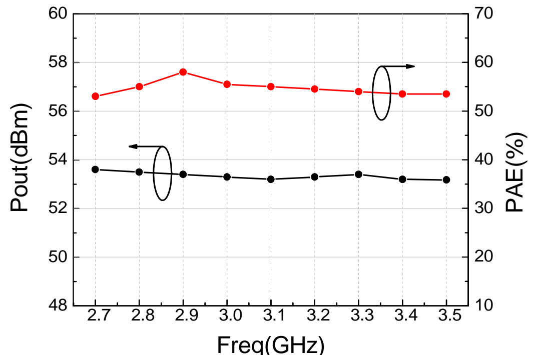
- ●Frequency：2.7~3.5 GHz
- ●Impedance 50Ω
- ●Metal Substrate
- ●Operating Temperature：-55 °C~+85 °C

Electrical Specification

Condition：50Ω，Vd=+28V，Vg= -5V；

（typical testing condition：1ms pulse width，duty cycle 10%）

Parameter	Unit	Standard	Typ. Value
Frequency	GHz	2.7~3.5	--
Pout	dBm	⩾53	53.5
Power Flatness	dB	⩽1	0.8
Power Gain	dB	⩾10	10.5
P.A.E	--	⩾50%	53%

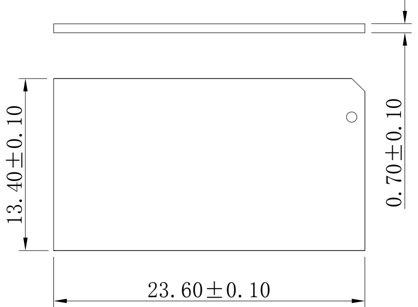


Limited Rating Value

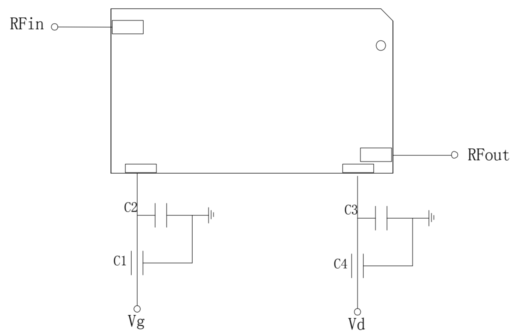
Power Supply：VDS+40V；VGS-10V

Storage Temperature：-65°C~+175 °C

Operating Temperature：-55 °C~+85 °C



Operating Remarks

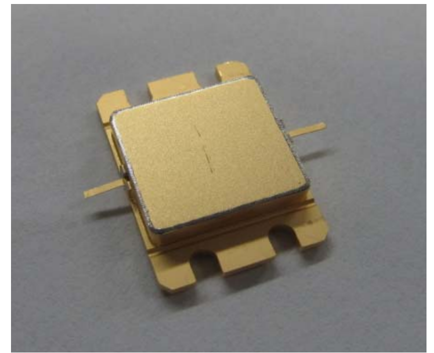


- ● CuMo Substrate is applied, SMA and substrate can also be provided.
- ● Connect the circuit according to left diagram. Well grounding and heat dissipation shall be applied.
- ● Power Filter and Storage Capacitor shall be well selected under Pulse operation.

2.7~3.0 GHz 200W Power Module **HEG616B**

HEG616B is a GaN Internally Matched Module based on our own GaN device with advanced flat internally matching technology/thin film integration technology. It can cover the frequency of 2.7-3.0 GHz, can be operating in both CW and Pulse condition.

Features

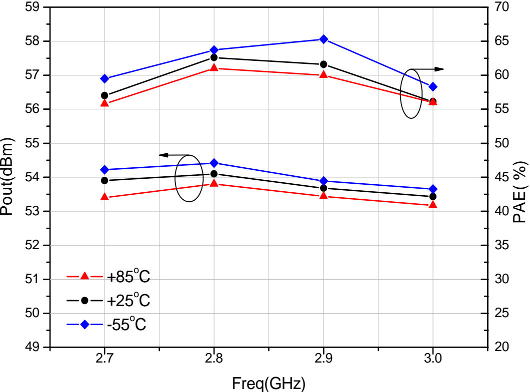


- ●Frequency：2.7~3.0GHz
- ●Impedance 50Ω
- ●Metal Package QF136P
- ●Operating Temperature：-55 ºC~+85 ºC

Electrical Specification

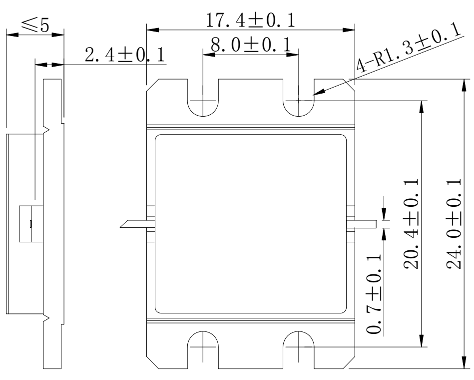
Condition：50Ω，Vd=+32V，Vg= -2.3V；（typical testing condition：3ms pulse width， duty cycle 10%）

Parameter	Unit	Standard	Typ. Value
Frequency	GHz	2.7~3.0	--
Pout	dBm	≥53	53.3
Power Flatness	dB	≤1.0	0.8
Power Gain	dB	≥11.5	12
P.A.E	--	≥55%	57%

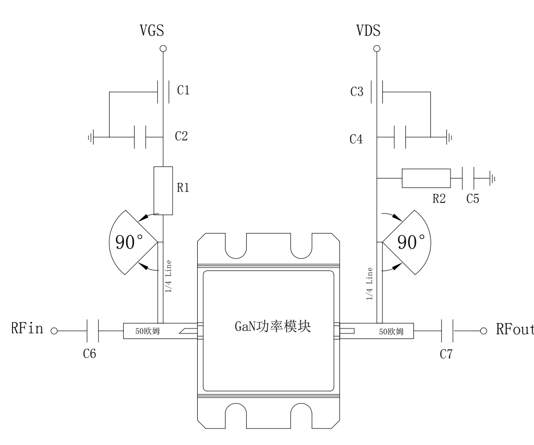


Limited Rating Value

Power Supply：V_{DS}+40V；V_{GS}-10V
Storage Temperature：-65ºC~+175 ºC
Operating Temperature：-55 ºC~+85 ºC

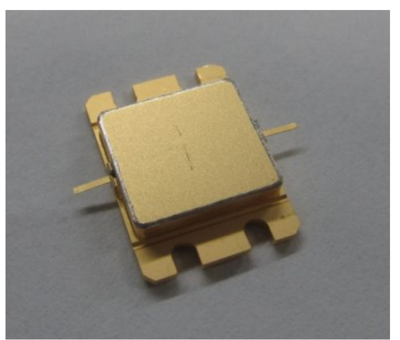


Operating Remarks



- ● Typical Package is metal package of QF136P, SMA and substrate can also be provided.
- ● Connect the circuit according to left diagram. Well grounding and heat dissipation shall be applied.
- ● Power Filter and Storage Capacitor shall be well selected under Pulse operation.

9.0~9.5GHz 100W Power Module
（Part Number：HEG625B）



Features:

- Frequency：9.0~9.5GHz
- 50Ω impedance matching, easy used in cascade.
- Package: QF136H
- Operation Temperature：-55~+85 ºC

Electrical Specification

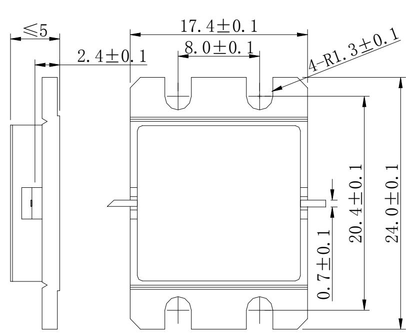
Operating Condition：50Ω test system，Vd=28V，Vg=-2.3V；
（Typical test condition：Pulse Width1ms，Duty cycle10％）

Parameter	Unit	Specification value	Typical values
Frequency	GHz	9.0~9.5	--
Psat	dBm	≥50	50.3
Power Flatness	dB	≤1.0	0.8
Power Gain	dB	≥8	8.3
P.A.E	--	≥38%	40%

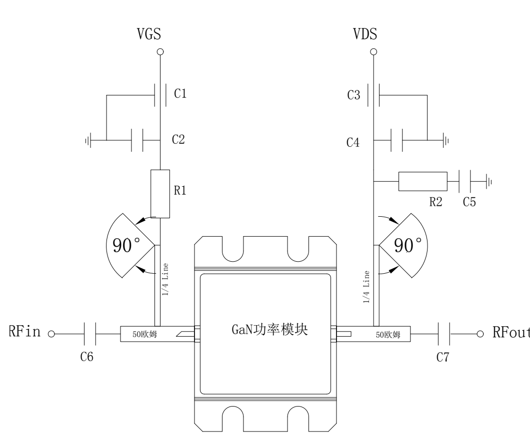
Note：The higher power, higher efficiency and wider band products can be customized

Limited Rating Values

Power Voltage：Vd: +40V；Vg: -10V
Storage temperature：-65ºC~+175 ºC
Operating Temperature：-55 ºC~+85 ºC



Application Instruction



Attention:

1, The typical package is QF136H, the SMA cassette package or carrier form can be provided according to the customers' requirements;

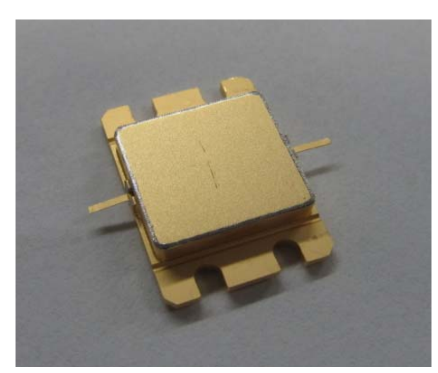
2, Circuit connected is according to the circuit diagram, and anti-static process should be attended. Good grounding and thermal conditions should be ensured when the power devices using;

3, Under the pulsed operating conditions, in order to ensure a good performance of the

power module. The power supply filter and energy storage capacitor capacitance value is reasonable selected according the modulation scheme and the corresponding requirements.

3.1~3.5 GHz 220W Power Module HEG803B

HEG803B is a GaN Internally Matched Module based on our own GaN device with advanced flat internally matching technology/thin film integration technology. It can cover the frequency of 3.1-3.5 GHz, can be operating in both CW and Pulse condition.



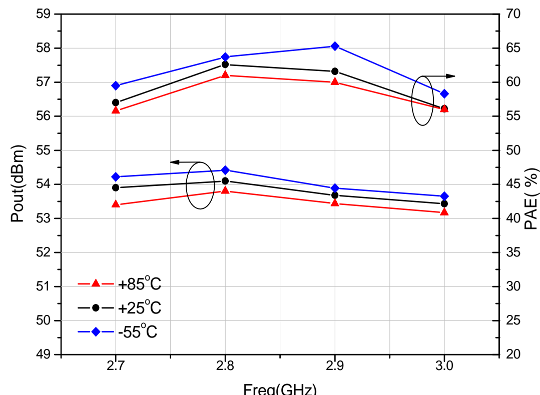
Features

- ●Frequency：3.1~3.5 GHz
- ●Impedance 50Ω
- ●Metal Package QF136P
- ●Operating Temperature：-55 ºC~+85 ºC

Electrical Specification

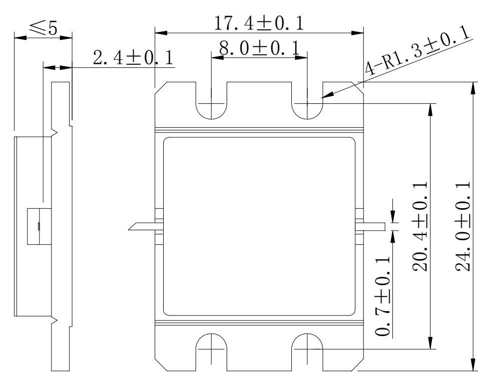
Condition：50Ω，Vd=+28V，Vg= -2.2V；
（typical testing condition：1ms pulse width，duty cycle 10%）

Parameter	Unit	Standard	Typ. Value
Frequency	GHz	3.1~3.5	--
Pout	dBm	≥53	53.5
Power Flatness	dB	≤0.5	0.3
Power Gain	dB	≥11	11.5
P.A.E	--	≥58%	60%

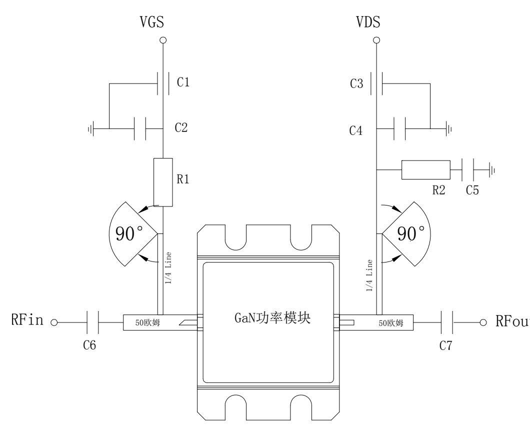


Limited Rating Value

Power Supply：V_{DS}+40V；V_{GS}-10V
Storage Temperature：-65ºC~+175 ºC
Operating Temperature：-55 ºC~+85 ºC



Operating Remarks



- ● Typical Package is metal package of QF136P, SMA and substrate can also be provided.
- ● Connect the circuit according to left diagram. Well grounding and heat dissipation shall be applied.
- ● Power Filter and Storage Capacitor shall be well selected under Pulse operation.

METDA Semiconductor

Number	
Pages	

测 试 报 告

TESTING REPORT

Product： 2.7-3.1GHz 250W GaN Transistor

Part Number： HEG813B

Standard： Testing Standard

METDA

Testing Record

Page Number 1

Product and Part Number	HEG813B, 2.7-3.1GHz 250W GaN Transistor			Group	——	
Testing Items	Electrical Specification		Environmental Condition		Temperature： 25 ℃ Humidity ： 35 %RH	
Measuring Instruments	8563E Spectrum Analyzer（390305-101）	Valid	2014.10.28～2015.10.27	Method	JY16.007-2014	
	Power Meter N1911A（350502-214）		2014.12.26～2015.12.25		JY16.005-2014	
	Vector Network N5242A（400801-282）		2015.03.02～2016.03.01		JY16.008-2014	
	E8257D Signal Source（380107-207）		2015.03.26～2016.03.25		JY16.010-2014	
Testing Standard	——					
Testing Condition	Frequency：2.7-3.1GHz；Pulse Width：1ms/3ms/6ms/10ms；Duty Cycle：5%/15%/30%/50%；Supply Voltage：**+32V**，-2.3V					

Number NO.1	Parameter		Unit	Frequency								
				2.7GHz	2.8GHz	2.9GHz	3.0GHz	3.1GHz				
				Testing Result								
1ms 5%	**Saturation (Pout)**	——	dBm	54.93	54.85	54.69	54.47	54.3				
	P.A.E (PAE)	——	%	55.3	59.2	61	58.8	55.2				
3ms 15%	**Saturation (Pout)**	——	dBm	54.85	54.8	54.65	54.4	54.2				
	P.A.E (PAE)	——	%	54.2	57	59.5	57.9	54.8				
6ms 30%	**Saturation (Pout)**	——	dBm	54.6	54.6	54.4	54.2	54				
	P.A.E (PAE)	——	%	54.1	55.4	58	56.3	53.3				
10ms 50%	**Saturation (Pout)**	——	dBm	54.1	54.2	54	53.8	53.5				
	P.A.E (PAE)	——	%	50.8	54	55.5	52.8	49.5				
Remarks												

Examiner：____________________ Date：____________

Testing Record

Product and Part Number	HEG813B, 2.7-3.1GHz 250W GaN Transistor	Group	——
Testing Items	Electrical Specification	Environmental Condition	Temperature： 25 ℃ Humidity ： 35 %RH

Measuring Instruments							
Measuring Instruments	8563E Spectrum Analyzer（390305-101）	Valid	2014.10.28～2015.10.27	Method	JY16.007-2014		
	Power Meter N1911A（350502-214）		2014.12.26～2015.12.25		JY16.005-2014		
	Vector Network N5242A（400801-282）		2015.03.02～2016.03.01		JY16.008-2014		
	E8257D Signal Source（380107-207）		2015.03.26～2016.03.25		JY16.010-2014		

Testing Standard	——
Testing Condition	Frequency：2.7-3.1GHz；Pulse Width：1ms/3ms/6ms/10ms；Duty Cycle：5%/15%/30%/50%；Supply Voltage：**+32V**，-2.3V

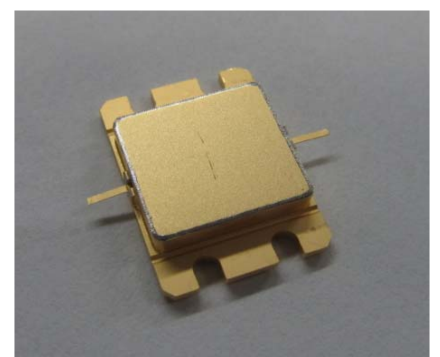
Number NO.2	Parameter		Unit	Frequency								
				2.7GHz	2.8GHz	2.9GHz	3.0GHz	3.1GHz				
				Testing Result								
1ms 5%	**Saturation (Pout)**	——	dBm	55.1	55	54.89	54.45	54.3				
	P.A.E (PAE)	——	%	56	59.8	59.8	56.8	53.5				
3ms 15%	**Saturation (Pout)**	——	dBm	54.95	54.85	54.8	54.3	54.23				
	P.A.E (PAE)	——	%	54.8	57.3	58	55.8	53				
6ms 30%	**Saturation (Pout)**	——	dBm	54.85	54.6	54.5	54.15	54.08				
	P.A.E (PAE)	——	%	54.5	55.9	56.4	53.2	51.5				
10ms 50%	**Saturation (Pout)**	——	dBm	54.2	54.3	54.1	53.85	53.36				
	P.A.E (PAE)	——	%	53.2	53.5	52.4	50.8	48.9				
Remarks												

Examiner：______________________ Date：______________

2.7~3.5 GHz 250W Power Module HEG813B

HEG813B is a GaN Internally Matched Module based on our own GaN device with advanced flat internally matching technology/thin film integration technology. It can cover the frequency of 2.7-3.5 GHz, can be operating in both CW and Pulse condition.

Features

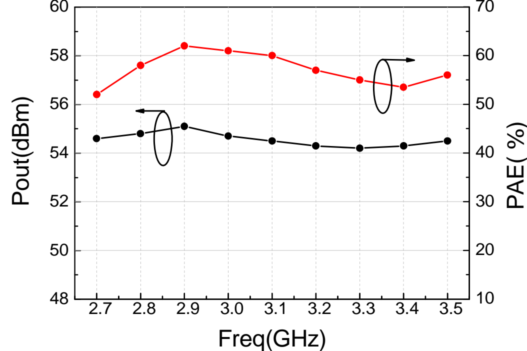


- ●Frequency：2.7~3.5GHz
- ●Impedance 50Ω
- ●Metal Package QF136P
- ●Operating Temperature：-55 ºC~+85 ºC

Electrical Specification

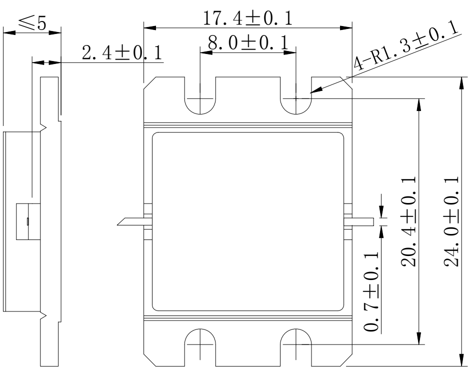
Condition：50Ω，Vd=+32V，Vg= -2.3V；
（typical testing condition：3ms pulse width，duty cycle 10%）

Parameter	Unit	Standard	Typ. Value
Frequency	GHz	2.7~3.5	--
Pout	dBm	≥54	54.3
Power Flatness	dB	≤1.0	0.8
Power Gain	dB	≥10	10.5
P.A.E	--	≥50%	55%

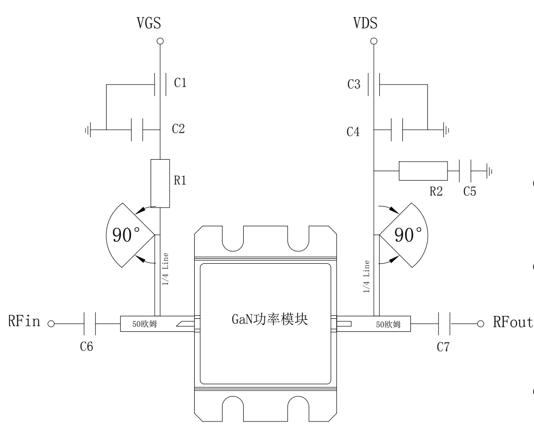


Limited Rating Value

Power Supply：V_{DS}+40V；V_{GS}-10V
Storage Temperature：-65ºC~+175 ºC
Operating Temperature：-55 ºC~+85 ºC



Operating Remarks



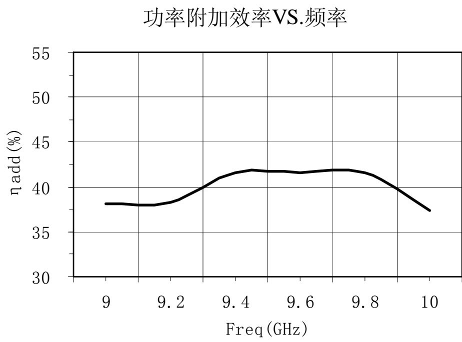
- ● Typical Package is metal package of QF136P, SMA and substrate can also be provided.
- ● Connect the circuit according to left diagram. Well grounding and heat dissipation shall be applied.
- ● Power Filter and Storage Capacitor shall be well selected under Pulse operation.

NC41610S-910P100
GaN Internally Matched Transistor,9.0-10.0GHz

Features:

- Frequency：9.0～10.0GHz
- Power Gain：8.0dB
- Output Power：50.0dBm
- P.A.E.：37%
- Packaging：QF136H

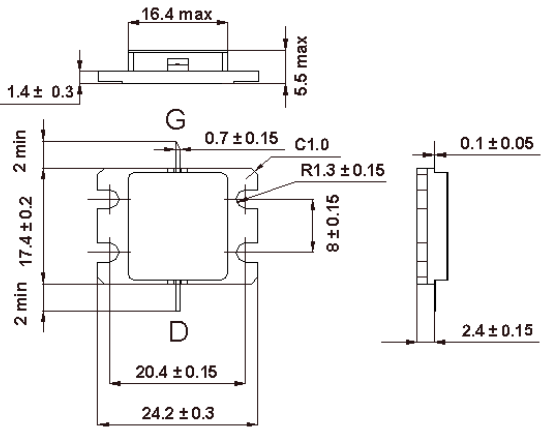
P.A.E. vs. Frequency



Electrical Specification（TC=25℃）

Parameter	Test Condition	Min.	Typ.	Max.	Unit
Output Power	f=9.0～10.0GHz VGS=-2.0～-3.0V VDS=+28V Pulse width：1ms Duty cycle：35%	50.0	-	—	dBm
Power Gain		8.0	-	—	dB
P.A.E.		37.0	-	—	%
Gain Flatness		—	—	1.0	dB
Pinch-off Voltage	VDS=+6V，IDS≤100mA	-4.0	—	-2.0	V
Negative I_{GS}	VDS=0V，VGS=-6V	—	—	5	mA

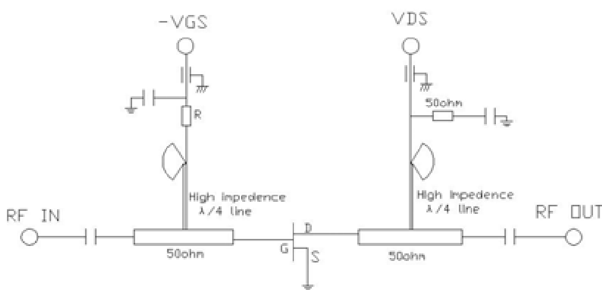
Dimension and Outline



Note: The unit is mm

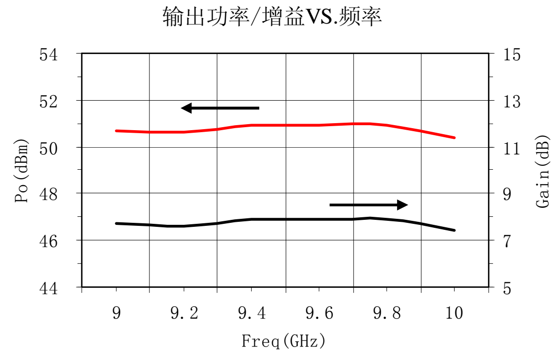
Limited Rating Values

V_{DS}	+32V
V_{GS}	-5V
Power Dissipation（T_C=25℃）	130W
Storage Temperature	-65℃～+175℃
Operating Temperature	-55℃～+85℃



Typical Testing Curves

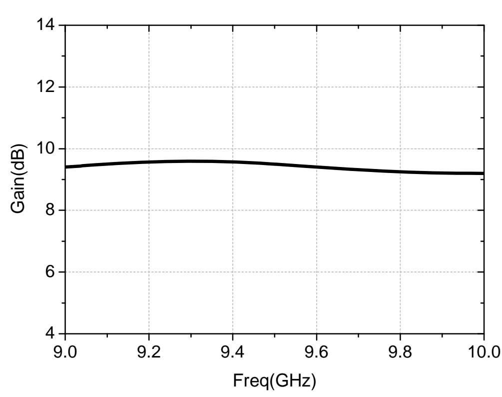
Po/Gain vs. Frequency



Features:

- Frequency：9.0-10.0GHz
- Power Gain：8.5dB
- Output Power：51.8dBm
- P.A.E：38.0%
- Packaging：QF136H

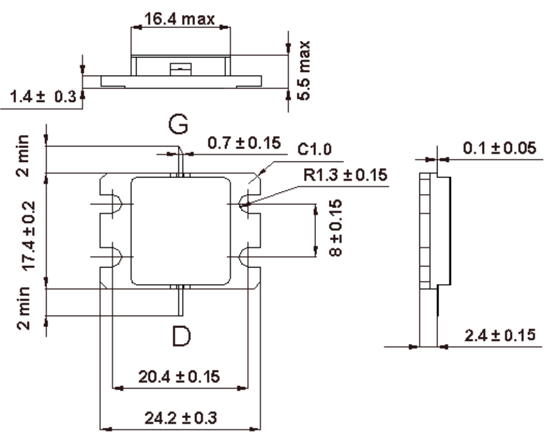
Power Gain VS. Frequency



Electrical Specification（TC = 25℃）

Parameter	Test Condition	Min.	Typ.	Max.	Unit
Output Power	f=9.0～10.0GHz V_{GS}=-1.0～-2V V_{DS}=32V I_{DS}=（0.2～0.5）I_{DSS} Pulse width 1mS，duty cycle 10%	51.8	-	-	dBm
Power Gain		8.5	-	—	dB
P.A.E.		38.0	-	—	%
Gain Flatness		—	—	1.0	dB
Pinch-off Voltage	V_{DS}=6V，I_{DS}≤100mA	-4.0	—	-2.0	V
Negative I_{GS}	V_{DS}=0V，V_{GS}=-10V	—	—	5	mA

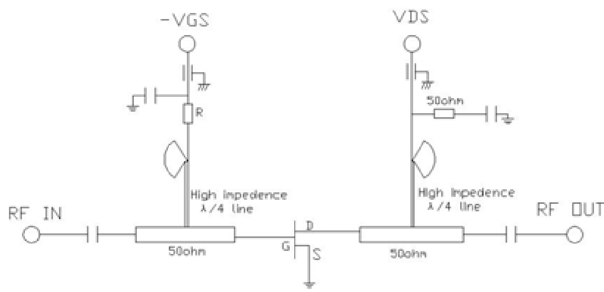
Dimension and Outline



Note: The unit is mm.

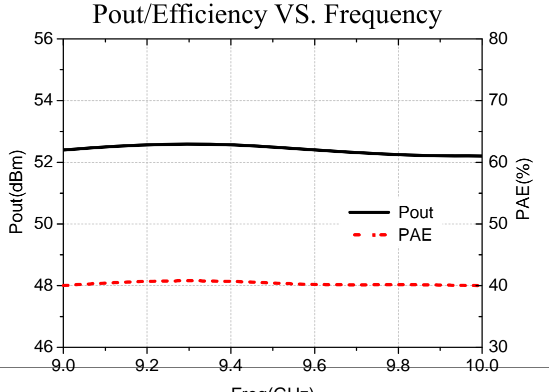
Limited Rating Values

V_{DS}	+44V
V_{GS}	-5V
Power Dissipation（T_C=25℃）	240W
Storage Temperature	-65℃～+175℃
Operating Temperature	-55℃～+85℃



Typical Testing Curves

Pout/Efficiency VS. Frequency



Attention

1)This device is internally matched device. The input/output impedance is 50Ω.