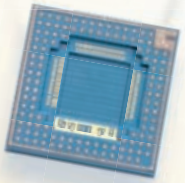


Precision thick film

Ceramics Design Guide

Offering innovative precision ceramic substrate solutions:

> Precision Thick Film
> High Performance Chip Resistors
> Advanced Etching Technology
> LTCC
> Lower-cost Microwave Circuits

LTCC

Tight tolerances

Anaren®

What'll we think of next?®

800-411-6596 > www.anaren.com

About this Product & Design Guide

This Product & Design Guide reflects the current capabilities of Anaren Ceramics' facility and experience. We've provided it to assist you in the initial evaluation of your design's compatibility with the various thick film and LTCC technologies we offer — as well as to introduce you to methods, processes, and techniques that can minimize costs and cycle times. This guide does not represent the full range of possibilities of our fast-expanding and continually improving technologies, nor does it replace the interaction between customers and Anaren Ceramics' engineers; this dialogue is welcome and needed to provide the most robust and cost-effective design.

About Us

Anaren Ceramics — Anaren Ceramics, a subsidiary of Anaren, is a leading manufacturer of quality thick film circuits. From multilayer substrates and LTCC, to lower-cost microwave circuitry featuring high-precision, etched conductors, chip resistors and attenuators, and more — Anaren Ceramics is your innovator in thick film processing. Our specialties include:

> **Exclusive, ceramic-based thick film and LTCC solutions.** Whatever your product requirements may be, we support a wide variety of the latest technologies and material, along with the engineering experience to utilize them adeptly and ingeniously. This enables us to provide solutions other suppliers simply can't.

  In the area of substrates, Anaren Ceramics' solutions include features such as filled substrate vias, edge wraps, integrated resistors, capacitors, and inductors. And throughout, we employ the latest thick film techology — and a variety of substrate materials such as alumina, aluminum nitride, beryllia, and ferrite for maximum design flexibility.

> **Vertical integration.** Need design assistance, ceramic machining, thick film screening, or LTCC manufacturing? How about etching, plating, laser trimming, and comprehensive product testing? Anaren Ceramics offers it all under one roof — for reduced costs, speedier turn times, and the advantages of shared information across disciplines.

> **Products for a diverse customer base.** At Anaren Ceramics, we work with customers in medical, wireless, optical, automotive, aerospace, aviation, and other industries.

  The varied and exacting demands of these sectors have made us proficient in developing all kinds of low-cost, quick-turn prototypes. They have also enabled us to compress our design-to-production cycle times; match our capacity to your low- or high-volume manufacturing needs; and develop a range of quality "stock" products, including microwave chip attenuators and the industry's smallest resistors meeting stringent performance standards.

> **The added confidence of Anaren engineering.** If your project calls for advanced microwave circuit design know-how or chip-and-wire assembly capabilities, in addition to Anaren Ceramics design expertise, count on our sister companies: Anaren Microwave, Inc. and MS Kennedy. Results can include reduced costs and time-to-market.

  So if you're thinking of solutions never before possible, think Anaren Ceramics! Start with this Product & Design Guide for data, specifications, and drawings — then call us at 603-898-2883 when you need the expertise, experience, and capabilities to make those solutions real.

Product Quality Assurance

> ISO-9001:2008 registered

> Quality requirements MIL-Q-9858

> QPL listed chip resistors MIL-PRF-55342

> Test capabilities MIL-PRF-38534

Contact

Anaren Ceramics, Inc.
27 Northwestern Drive
Salem, NH 03079
Tel: 603-898-2883
Fax: 603-898-4273
E-mail: ceramics@anaren.com
www.anaren.com/Ceramics

Table of Contents

Thick Film Materials

Highlights

- > Sequentially applied layers of alternating conductor and dielectric to build up the multilayer structure
- > Typically used for one to eight conductor layers per side (single or double sided)
- > A selection of metals for wirebonding, soldering, brazing
- > Integrated resistors, capacitors, inductors
- > Alumina, ferrite, aluminum nitride, beryllia substrates, and more
- > Wide range of resistor materials and values on a single substrate
- > Wraps and metallized substrate vias
- > Advanced substrate machining, including various shapes and cutouts
- > Combine with etched thick film and LTCC if needed
- > For recommended materials selection, please contact Anaren Ceramics for details

Conductors

Fritless golds are used for high-reliability conductors and for gold wire bonding. Fritted gold metallizations have higher adhesion to the substrate and, for that reason, are often substituted for fritless gold. Pt/Au and Pt/Pd/Au alloys have very high solder leach resistance and are used for critical solderable applications. Pure silvers have the lowest resistivity, and when alloyed with palladium and/or platinum, become increasingly leach resistant. Careful silver alloy selection will produce a high-reliability part in cost-sensitive applications. Special acid-resistant alloys of silver are used as the base metal for nickel barrier plating when the ultimate in solder leach resistance is required.

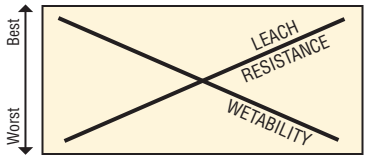


Table 1.2.1: Conductor Properties

	Gold	Platinum/ Gold	Silver	Palladium/ Silver
Relative Cost[1]	20-25	25-30	1	2-5
Sheet Resistivity (MΩ/sq)	3-7	60-100	1-2	10-50
Solderability (Sn/Pb)[2]	4	2	5	2-4
Leach Resistance[2]	1	5	1	3-4
Printed Typical Fired Thickness (microns/layer)	7-13	10-15	10-18	10-25
Typical Min. Line Width (width in mils)	5-7	7-10	7-10	7-10
Etched Thick Film Min. Line Width (width in mils)	0.8		2	
Typical Etched Fired Thickness (microns/layer)	6-12		10-14	

[1] Relative Cost: 1 = Best
[2] Relative Values: 5 = Best

Dielectric

Thick film dielectrics are designed to be used as insulators between conductor layers in crossover and multilayer applications. Overglazes are used as protective coatings over printed resistors and capacitors. They also serve as solder stops in surface mount assemblies and provide protection from harsh chemicals in the plating process.

Table 1.3.1: Dielectric Properties

	Dielectric Constant	Dissipation Factor	Breakdown Voltage (V/mil)	Fired Thickness (microns)	Insulation Resistance (ohms)
Dielectric	6-12	< 0.5%	500	38-51	$>10^{11}$ @ 100 V
Low - K	3.9-4.5	<0.01% 0.04% @ 20 GHz	500	25-51	$>10^{11}$ @ 100 V

* Contact Anaren Ceramics for recommendations.

Resistors

Standard resistor materials are made from glasses and metal oxides of ruthenium metal. Sheet resistivities are available from milliohms to gigaohms and can be combined on a single substrate. Standard trim tolerances are 10% through 1%, and in some cases to 0.5%. Large numbers of minimum size resistors on a substrate may limit the tolerance to 5% to 10% due to yield considerations.

Table 1.4.1: Typical Resistor Characteristics

	Sheet Resistivities (ohms/square)							
	1	10	100	1K	10K	100K	1M	10M
TCR (PPM/C) Maximum	±300	±300	±300	±300	±300	±300	±300	±300
Typical	100±200	100±200	100±200	0±200	0±200	0±200	0±200	0±200
Maximum Rated Power Dissipation (mW)								
Alumina	500	575	750	500	400	275	100	10

Note: Laser trim will reduce resistor area by up to 50%, power based on 1306 metric size.

VCR

If VCR is important in your application, contact Anaren Ceramics for design and material recommendations.

Capacitors

Capacitors are processed using standard screen printing techniques and fired directly onto any layer of the substrate. They may also be buried within or on top of multilayer structures. Electrodes must be of the same material. Typical dielectric thickness is 40 microns. Capacitor tolerance is typically ± 30%. Design options are available to reduce tolerances.

Table 1.6.1: Typical Printed Capacitor Dielectric Properties

Dielectric Constant (K)	20-50	100-300	500-750	750-1500
Dissipation Factor (1 kHz)	< 0.3%	< 1.0%	< 1.2%	< 3%
Dissipation Factor (1 MHz)	< 0.5%	< 1.6%	< 2.0%	–
Dielectric Strength (Volts/mil)	> 500	> 500	> 500	> 500
Insulation Resistance (@ 100 V, 1 kHz)	> 10^{11}	> 10^{11}	> 10^{11}	> 10^{9}
TCC (25°C-125°C)	< 3%	< 6%	< 15%	(Z5U)

Note: Typical properties based on 0.100" x 0.100" capacitor: Contact Anaren Ceramics for more details

Substrates

Standard substrate materials include alumina (Al_2O_3) in sizes to 6" x 4", aluminum nitride (AlN) in sizes to 4" x 4", and beryillia (BeO) in sizes to 2.3" x 2.9". Laser scribing 0.025"-thick rectangular alumina provides the most effective approach to meeting mechanical requirements. When necessary, substrates can be machined to produce virtually any outline. Other available substrate materials include barium titanate, ferrite, and quartz. Standard thicknesses 10 to 120 mils ±10%. Standard camber 3 mils/inch. Increased control of thickness, camber, and surface finish is available by lapping or polishing.

Table 1.7.1: Substrate Material Characteristics

	Unit	96% Alumina	99.5%/ 99.6% Alumina	Beryllia (BeO)	Aluminum Nitride (AlN)
Dielectric Constant (1MHz)		9.5	9.9	6.5	8.6
Dissipation Factor (1MHz)		0.0004	0.0001	0.0004	0.001
Thermal Conductivity (100°C)	W/m-K	20	27	270	170
Coeff. Thermal Expansion	ppm/°C	6.3-8.0	7.0-8.3	9.0	4.6

Table 1.7.2: Thicknesses and Sizes (BeO/AlN)

	Standard Thickness (mils)									
	10	15	20	25	40	50	60	80	100	120
Alumina	X	X	X	X	X	X	X	X	X	X
BeO	X	X	X	X	X		X			
AlN	X	X	X	X	X	X	X			

Table 1.7.3: Recommendation for attach methods

	SnPb Solder	Epoxy	RoHS (Pb Free)	SAC Solder	AuSn Solder	Au Wire-bond	Al Wire-bond
Au		X			X	X	X
Pt-Au	X	X	X	X	X	X	
Ag		X					X
Pt-Ag	X	X	X				
Electroless Nickel-Gold	X	X	X	X	X	X	X
SnPb Plate	X		X	X			
Matte Tin Plate	X		X				

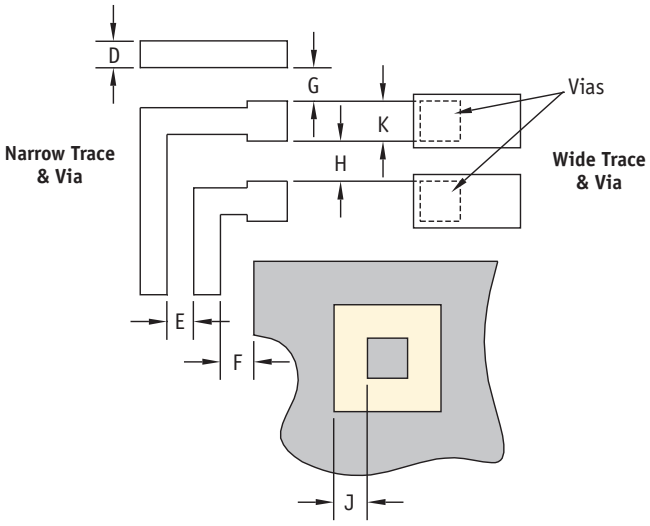
Design Features

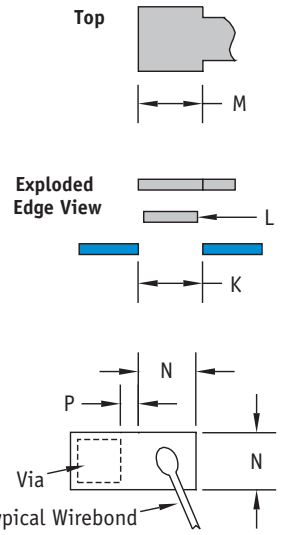
Thick film multilayer design rules follow on the next several pages.

> Minimum and standard feature sizes are shown. All features can be of greater size unless otherwise indicated.

> Feature sizes greater than the minimum improve producibility.

Conductors & Vias



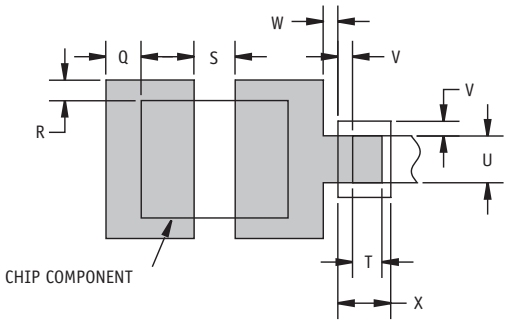


	Rule	Etched Gold Minimum (mils)	Etched Gold Standard (mils)	Standard Thick Film Minimum (mils)	Standard Thick Film Standard (mils)
D	Conductor Width	0.8	1.3	7	10
E	Conductor Spacing	0.8	1.3	7	10
F	Conductor Spacing Different Materials	6	12	6	12
G	Conductor to Via	8	10	10	12
H	Via to Via, Isolated	10	15	12	15
J	Conductor Isolation in Power/Ground Plane	7	10	10	12

	Rule	Etched Gold Minimum (mils)	Etched Gold Standard (mils)	Standard Thick Film Minimum (mils)	Standard Thick Film Standard (mils)
K	Via Diameter	2.0	4.0	8	10
L	Via Fill[1]	2.5	N/A	7	9
M	Conductor Over Via[2]		3.5 x 3.5	10 x 10	15 x 15
N	Wirebond Pad Size (for 1 mil Gold Wire)		5 x 5	10 x 10	10 x 15
P	Via to Wirebond Pad[3]	12	15	12	15

[1] Via fill typically ½ mil smaller than via opening all around
[2] Minimum size same as via size
[3] This spacing improves planarity of wirebond site

Solder Pads & Gold/Silver Interface

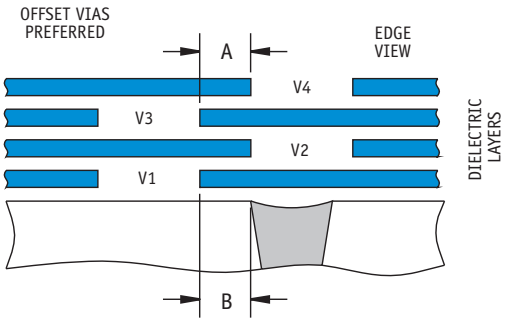


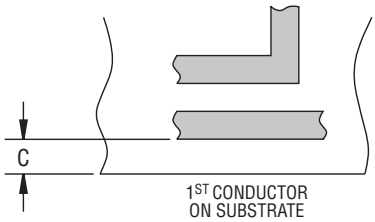
	Rule	Minimum (mils)	Standard (mils)
	Rules Q-S: Solder Pads[1]		
Q	Chip Pad Extension, Length	10	12
R	Chip Pad Extension, Width	5	7
S	Solder Pad Spacing	15	–
	Rules T-X: Au-Ag Interface where required[2]		
T	Overlap Length, Dissimilar Materials	8	12
U	Overlap Width, Dissimilar Materials	10	12
V	Solder Mask Overlap at Gold-Silver Interface	5	7
W	Glaze Solder Mask Stepback	2	5
X	Glaze Width	8	15

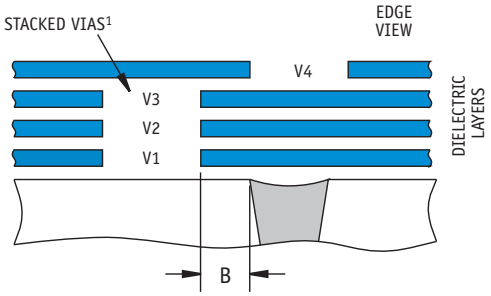
[1] Suggested dimensions for typical components
[2] Non-alloyed gold must be protected from the leaching effects of solder

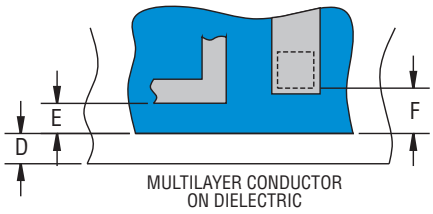
Design Features *(continued)*

Vias, Dielectrics & Crossovers





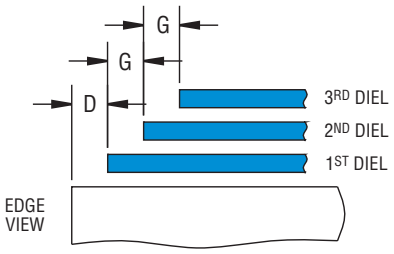


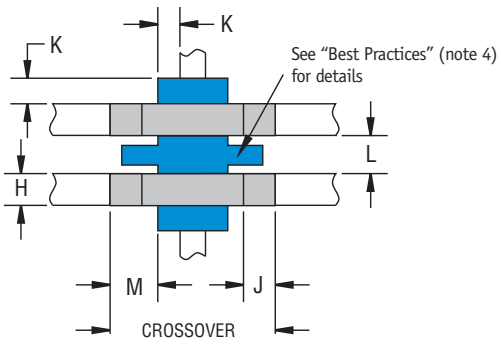


	Rule	Minimum (mils)	Standard (mils)
A	Offset Via Spacing	5	10
B	Via to Filled Substrate Hole	3	5

[1] Limit stacked layers to 3 before offsetting

	Rule	Minimum (mils)	Standard (mils)
C	Conductor to Snapped Substrate Edge Conductor to Diced Substrate Edge	8 2	10 5
D	Dielectric to Snapped Substrate Edge Dielectric to Diced/Machined Substrate Edge	8 0	10 5
E	Multilayer Conductor to Dielectric Edge	7	10
F	Via to Dielectric Edge	10	15



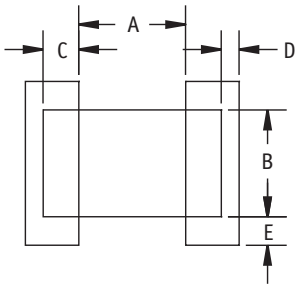


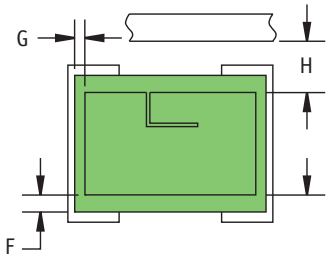
	Rule	Minimum (mils)	Standard (mils)
	Rules H-M also apply to conductors running off the edge of a dielectric		
G	Dielectric Stepback	0	2
H	Crossover Width	10	12
J	Crossover Overlap	8	12
K	Dielectric Overlap	7	10
L	Crossover Spacing	10	12
M	Crossover Length Beyond Dielectric	8	15

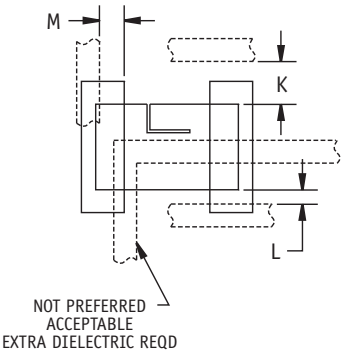
Note: A minimum of two layers of dielectric is needed for isolation between conductor traces. Dielectric layer counts greater than 4 may impact listed dimensions.

Design Features *(continued)*

Printed Resistors

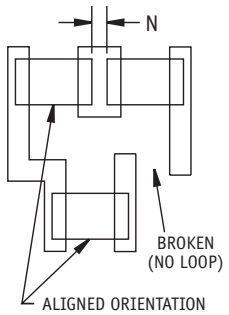




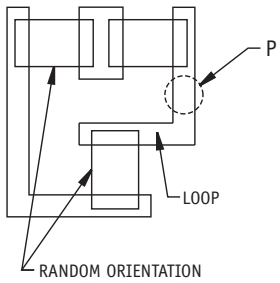


	Rule	Minimum (mils)	Standard (mils)
A	Resistor Length[1]	15	30
B	Resistor Width	15	30
C	Resistor/Termination Overlap	7	10
D	Termination Extension (Length Direction)	3	5
E	Termination Extension (Width Direction)	5	8
F	Overglaze Coverage, Width[2]	5	8
G	Overglaze Coverage, Length	0	3
H	Conductor to Resistor Edge	10	15
	Rules K-N apply to 1ST layer below resistor		
K	Buried Conductor to Resistor Along Termination	15	20
L	Buried Conductor to Untrimmed Resistor Edge	0	5
M	Buried Conductor to Trimmed Resistor Edge	10	15
N	Resistor to Resistor on Common Termination[3]	0	10
P	Resistor Probe Pad[4]	8 x 10	15 x 15
–	Resistor Orientation[5]	Random	Aligned
–	Resistor Loops[6]	Loop	No Loops

[1] Dimensions based on Au terminated resistors; Ag terminated add 10 mils
[2] Overglaze used where environmental stability is required
[3] Zero spacing allowed if both resistors use same paste
[4] Probe pad not covered by glaze or dielectric; located anywhere on trace; not in area reserved for termination extension; see E for reference
[5] Orienting resistors in the same direction is especially helpful for small-geometry resistors
[6] Identify resistor loops in drawing notes: contact Anaren Ceremics for details.



PREFERRED



ACCEPTABLE

Trim

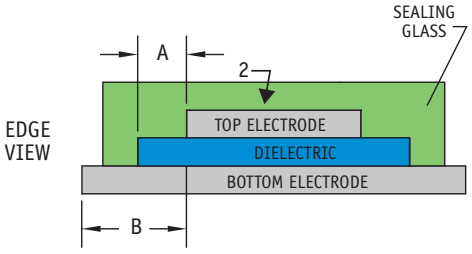
J-Cut
- Low Cost
- Improved Power performance
- Better RF performance

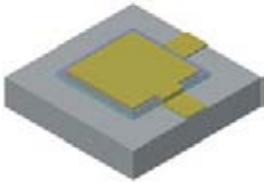
L-Predict Cut
- Best Tolerance performance
- Highest processing cost

Scan Cut
- Best Power performance
- Better Tolerance performance
- High processing cost

Note: Unless otherwise specified by customer, Mil STD 38534 and Mil STD 883 will be employed.

Printed Capacitors



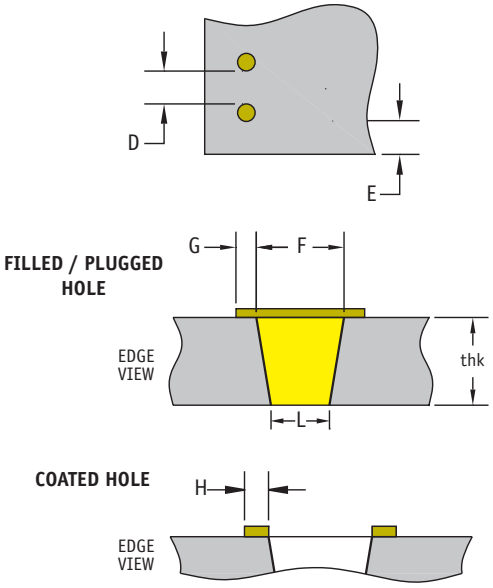


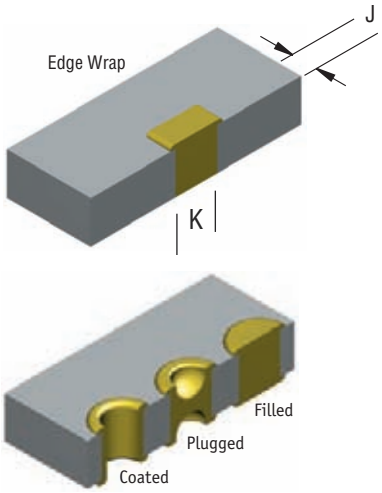
	Rule	Minimum (mils)	Standard (mils)
A	Dielectric Overlap Smaller Electrode	7	10
B	Larger to Smaller Electrode Overlap	2	5
	Value[1] 2pF to 500pF		
	Capacitor Tolerance	± 30%	± 50%

Note: Bottom and top electrode can be interchanged
[1] Value depends on Dk and area of capacitor
[2] Full encapsulation of sealing glass to prevent environmental exposure

Design Features *(continued)*

Holes and Edge Wraps





	Rule	Minimum	Standard
D	Hole Spacing (Edge to Edge)	Sub Thk	1.5 x Sub Thk
E	Hole Edge to Snapped Substrate Edge	1.0 x Sub Thk	
E	Hole Edge to Diced Substrate Edge	0.5 x Sub Thk	1.0 x Sub Thk
-	Substrate Length & Width Tolerance, Diced Edge	± 1 mil	± 2 mils
-	Substrate Length & Width Tolerance, Snapped Edge	± 5 mils	± 10 mils

Table 2.7.1: Hole Machining

	Rule	Minimum	Standard
L	Top Hole Diameter	10-25 mils thk	F-(thk x 10%)
L	Top Hole Diameter	30-40 mils thk	F-(thk x 10%)
L	Top Hole Diameter	50-60 mils thk	F-(thk x 10%)

	Rule	Minimum (mils)	Standard (mils)
F	Plugged/Filled Hole Diam, 10-25 mil thk Substrate	7	
F	Plugged/Filled Hole Diam, 30-40 mil thk Substrate	8	
F	Plugged/Filled Hole Diam, 50-60 mil thk Substrate	10	
G	Conductor Pad Covering Filled Hole	5	7
H	Annular Ring around Coated Hole	7	10
J	Wrap onto Top or Bottom Surface	15	20
K	Width of Edge Wrap	10	15
L	Bottom Hole Diameter	F-(thk x 10%)	

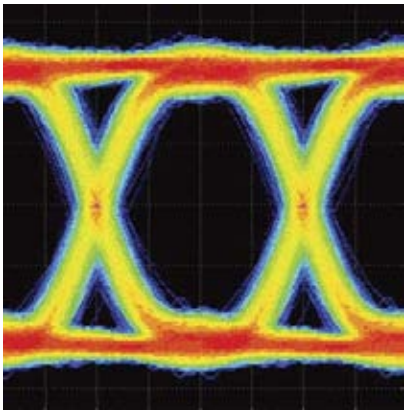
Note: Plugged and filled hole diameters should not exceed the ceramic thickness

Customer Drawings and CAD Files

> For any design work (thick film multilayer, etched thick film, or LTCC), customer CAD files are preferred in one of the following formats:
  – Gerber files preferred
  – AutoCad .DWG
  – DXF
> High-density designs require a customer-furnished netlist:
  – IPC 356D preferred
> All specifications should be listed on drawing or supporting documentation.
> In all cases, an active dialogue between you and your Anaren Ceramics team ensures that design requirements and applications intents are met!

Advanced Precision Etched Circuit Substrates (APECS)

For extremely tight tolerances at highly affordable prices ... Engage Anaren: Precision Etch Circuits



Anaren Ceramics Precision Etch Technology is your choice for RF/microwave circuits, filters, inductors and couplers.

- > Thin Film performance at Thick Film cost – up to 40% savings over Thin Film
- > Fine line capability: 1 mil lines, 1 mil spaces & better
- > Excellent line edge definition
- > Au and Ag etch capability
- > Integrates with standard Thick Film resistors & capacitors
- > Multiple substrates available: Alumina, AlN, BeO & more
- > No Nickel barrier means less intermodulation distortion
- > RoHS/REACH Compliant

The APECS process can be combined with standard thick film technology to create a highly integrated, more cost effective solution and improve overall substrate yield. Just use APECS precision lines and spacing in those distinct locations of your design where precision is needed most—leaving other, less precise areas on your substrate to be rendered using traditional thick film techniques. Want to integrate components? That's easy, too, because APECS substrates allow you to embed precision resistors, Lange couplers, and capacitors into the substrate itself — rather than applying discrete components using more labor-intensive, less consistent traditional component mounting approach.

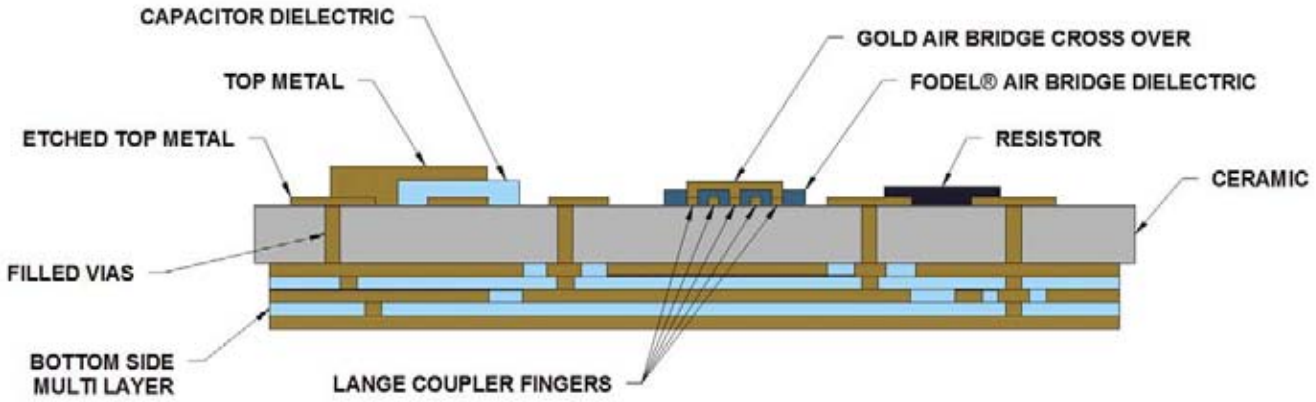


Figure 3.1.1: Cross-Section of APECS Circuit

Showing multilayer backside and integrated passives

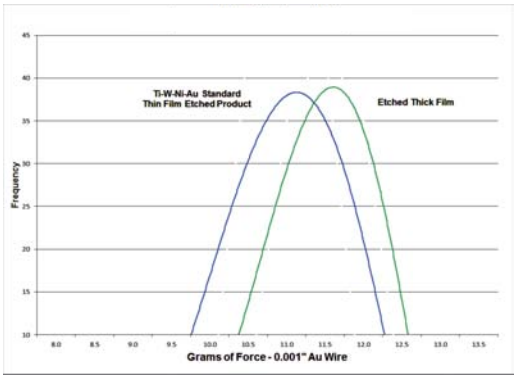


Figure 3.1.2: Comparative Wire Bond Data

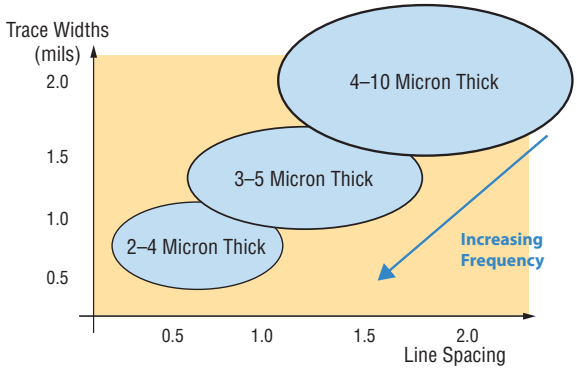


Figure 3.1.3: Relative Etch Window Capability

Advanced Precision Etched Circuit Substrates (APECS) *(continued)*

Etched Thick Film Capabilities

- Capacitors, resistors, hole fill, wraps, solder- and braze-metallizations
- Alumina (96%, 99.5%, 99.6%), ferrite, aluminum nitride, Beryllium Oxide and Quartz substrates
- Standard and low-K dielectrics
- Air bridges
- Multilayer structures
- Wide range of resistive values (0 to Gohm)
- Glass encapsulations

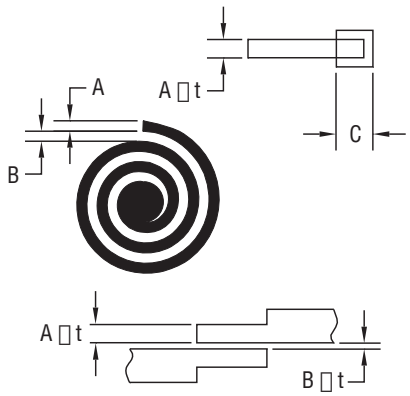


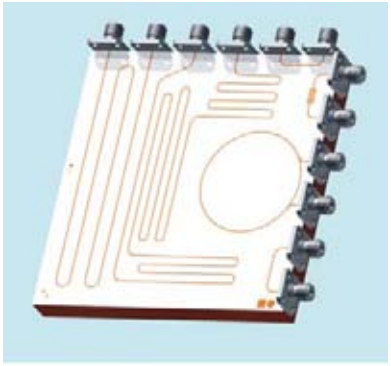
Figure 3.2.1: Etched Conductors

	Rule	Minimum (mils)	Standard (mils)
A	Conductor Width	0.8	1.3
t	Line Width Tolerance	± 0.1	± 0.2
B	Conductor Spacing Same Print Mask	0.8	1.3
C	Via Size Diameter (Photo Imaged Dielectric)	2	3

Note: For best tolerances, a lapped ceramic surface may be required.

The APECS RF Advantage

Comparing line losses between an APECS Thick Film board and a typical Thin Film board the line loss is significant lower for the APECS Thick Film. As the frequency increases the lower loss becomes even more significant. Both boards were fabricated using a 96% Alumina ceramics and identical Gold trace thickness.



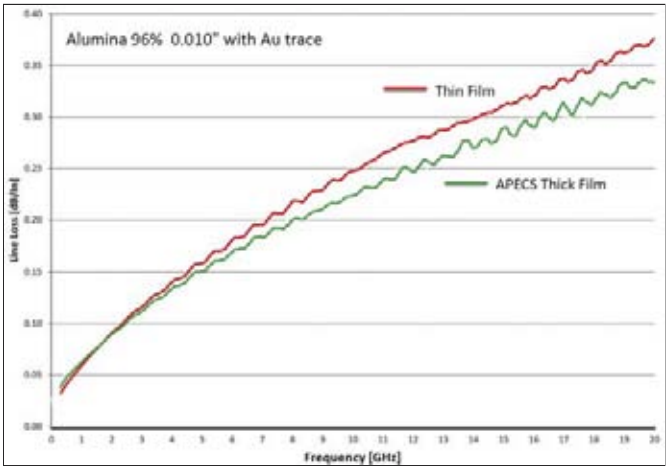
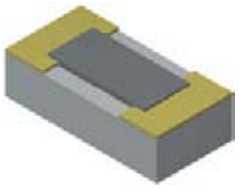


Figure 3.3.1: Line Loss Comparison APECS Thick Film vs. Thin Film

Chip Resistors

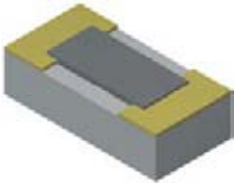
Style 1: Top contact, no wrap

Pads on resistor side only; use with wire-bonding



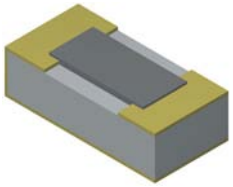
Style 2: Dual wrap

Common surface mount style; both terminations wrap around from resistor side to backside; solder or epoxy attach



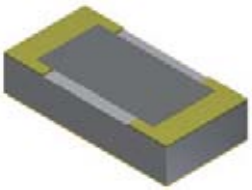
Style 3: Single wrap

One termination wraps from resistor side to full coverage on backside; attach wire to the other termination; use as a terminator or to increase thermal contact



Style 4: Top contact ground plane

Pads on the resistor side only; use with wire-bonding; backside conductor for improved thermal contact and consistent RF performance.



Listed on the following page are some of the more common chip sizes, styles, and terminations that Anaren Ceramics provides. If you do not find what you're looking for, call with your particular needs!

> **Sizes as small as** 20 x 10 mils (0.5 x 0.2 mm).

> **Wide resistance range,** from approximately 0 Ω to 50 GΩ. There are some limitations on size, tolerance, and TCR at the ends of these ranges.

> **Tolerance to 1%,** with tolerances to 0.1% available in some instances.

> **Anaren Ceramics is QPL listed** per MIL-PRF-55342. See the QPL or call for specifics.

> **VCR of .02 ppm** per volt can be achieved

> **Termination materials** include:

- Gold for wirebonding.
- Platinum-gold, palladium-silver for soldering or conductive epoxy attachment.
- Tin-lead plate, matte-tin, and electroless nickel and gold plate for soldering.
- Optional solder bumping.
- In addition to plating options, solder can be added to mounting surfaces.

> **Solders** include: Tin Lead, Gold Tin, Indium-based solders, and SAC solders (see table 1.7.3).

> **RF Resistors** up to 40 GHz available.

> **Higher frequency designs** are available.

> **Hi-rel processing is also available.**

Table 4.1.1: Chip resistor sizes and specifications (use metric size for ordering)

Inch size code	Length (inch)	Width (inch)	Metric size code	Length (mm)	Width (mm)	Power (W) T_a=70°C	Voltage (V)
0201	0.020	0.010	0502	0.50	0.20	0.040	40
0202	0.020	0.020	0505	0.51	0.51	0.050	40
0302	0.030	0.020	0805	0.76	0.51	0.060	40
0402	0.040	0.020	1005	1.02	0.51	0.080	40
0502	0.050	0.025	1306	1.27	0.64	0.125	40
0504	0.050	0.040	1310	1.27	1.02	0.200	40
0505	0.050	0.050	1313	1.27	1.27	0.250	40
0603	0.060	0.030	1508	1.52	0.76	0.180	48
0705	0.075	0.050	1913	1.91	1.27	0.280	60
0805	0.080	0.050	2013	2.03	1.27	0.280	60
1005	0.100	0.050	2513	2.54	1.27	0.375	80
1010	0.100	0.100	2525	2.54	2.54	0.750	80
1206	0.125	0.065	3217	3.18	1.65	0.600	100
1505	0.150	0.050	3813	3.81	1.27	0.560	120
2010	0.200	0.100	5125	5.08	2.54	1.500	160
2512	0.250	0.125	6432	6.35	3.18	2.300	200

Table 4.1.2: Available Termination Materials and Codes

Resistor Pad (F)	Back Pad (B)	Style 1	Style 2	Style 3	Style 4	Application
Au		A	G	G	G	WB, EP
Pt-Au		B	H	H	H	SO
Pd-Ag		C	L	L	L	SO, EP
Sn-Pb plate		D	J	J	J	SO
ENiG plate		P	K	K	K	WB, SO, EP
Matte Sn plate		T	N	N	N	SO
Au	Pt-Au			E	E	FWB, BSO
Au	Pd-Ag			F	F	FWB, BSO, BEP
AuSn bump		U			U	SO
Sn96 bump		W			W	SO
SnPb bump		X			X	SO

Key: WB = Wirebondable FWB = Front Wirebond SO = Solderable BSO = Back Solderable EP = Eposy BEP = Back Epoxy

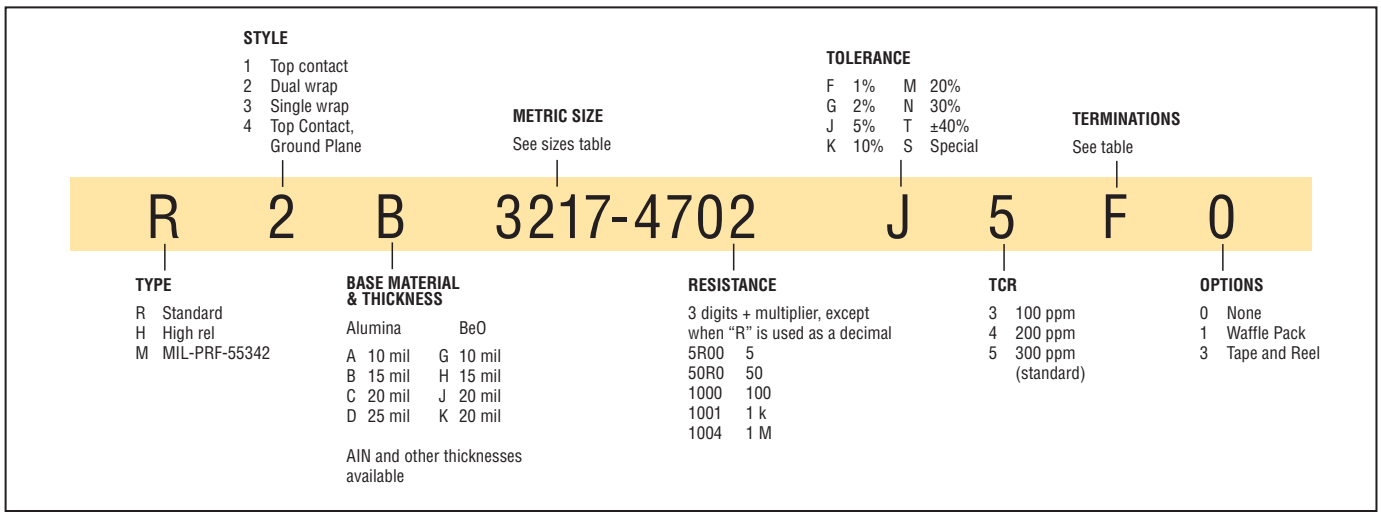
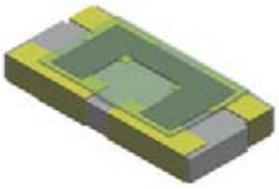


Figure 4.1.1: Part Numbering

Chip Attenuators

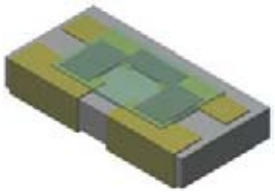
Style A: Dual wrap I/O pads

Attenuator (pi-pad) with wrap-around I/O's and grounds for solder or epoxy attach



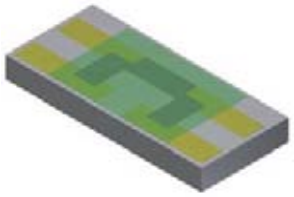
Style P: Top contact I/O with ground wrap

Attenuator with wirebond I/O pads and wrap-around grounds for solder or epoxy attach



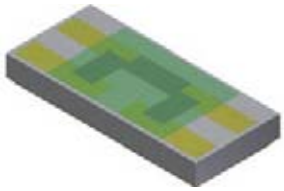
Style T: Top contact, no ground wrap

Attenuator with wirebond I/O pads and ground for epoxy attach



Style D: Top contact, no wraps, ground plane on back side

Attenuator with wirebond I/O pads and ground for solder or epoxy attach



Anaren Ceramics' attenuators are summarized as follows. If you do not see what you require, please do not hesitate to contact us to explore alternative solutions that may suit your particular needs!

> Characterized to 18 GHz

> Rated 0.125 W, 25 V at T_a = 70°C

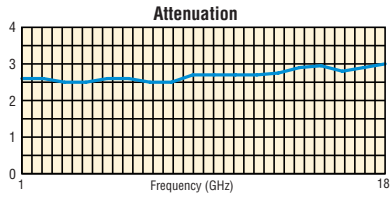
> Termination materials include:

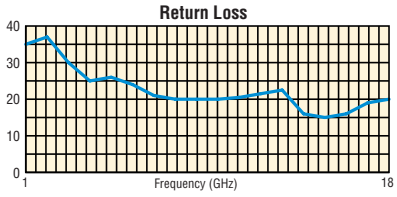
- Gold for wirebonding
- Platinum-gold, palladium-silver for soldering or conductive epoxy attachment
- Tin-lead plate, Matte-tin plate, gold plate for soldering. These terminations consist of three layers: a plateable silver, a solderable nickel barrier layer, and the outer plated layer.
- Optional solder tinning. In addition to the plating options, a relatively thick printing of solder (tin-lead or gold-tin) can be added on the mounting surface only.

> Hi-rel processing is also available.

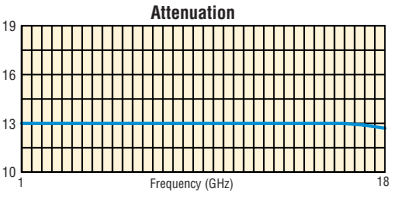
Typical Performance Data

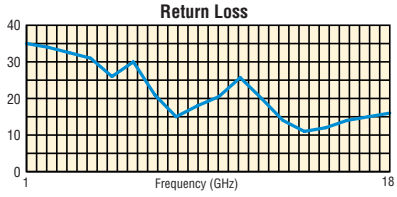
2.5 dB



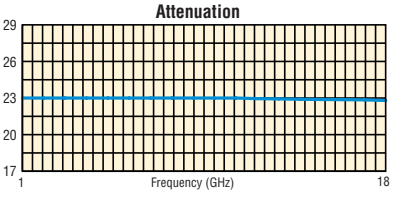


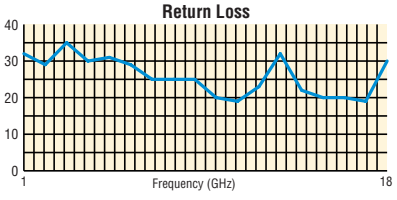
13 dB





23 dB





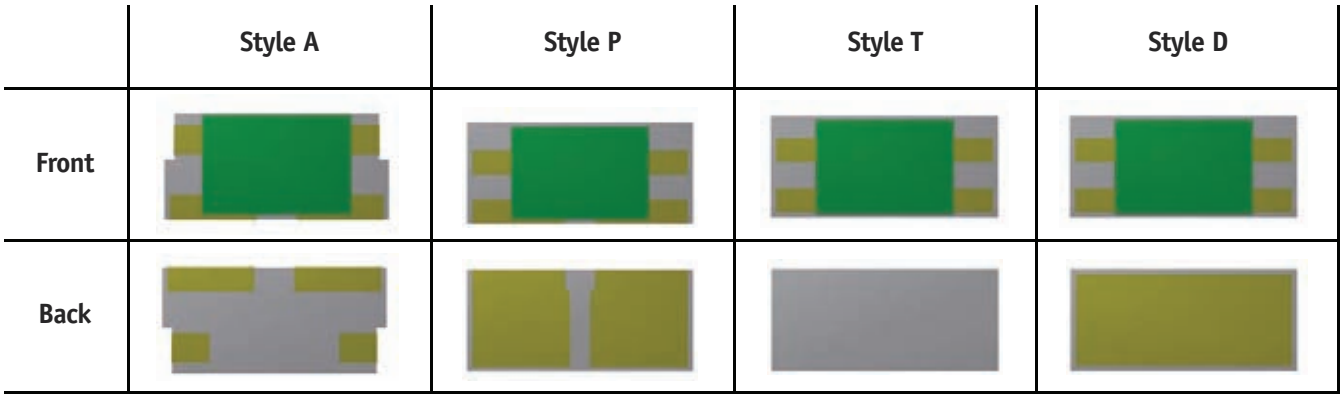


Figure 6.4.1: Chip attenuator sizes A (use metric size for ordering)

Table 5.1.1: Available Termination Materials and Codes

I/O (F)	Back Side Ground (B)	Style A	Style P	Style T	Style D	Application
Au		A	G	G	G	WB, EP
Pt-Au		B	H	H	H	SO
Pd-Ag		C	L	L	L	SO, EP
Sn-Pb plate		D	J	J	J	SO
ENiG plate*		P	K	K	K	WB, SO, EP
Matte Sn plate		T	N	N	N	SO
Au	Pt-Au			E	E	FWB, BSO
Au	Pd-Ag			F	F	FWB, BSO, BEP
AuSn bump		U				SO
Sn96 bump		W				SO
SnPb bump		X				SO

Key: WB = Wirebondable FWB = Front Wirebond SO = Solderable BSO = Back Solderable EP = Epoxy BEP = Back Epoxy

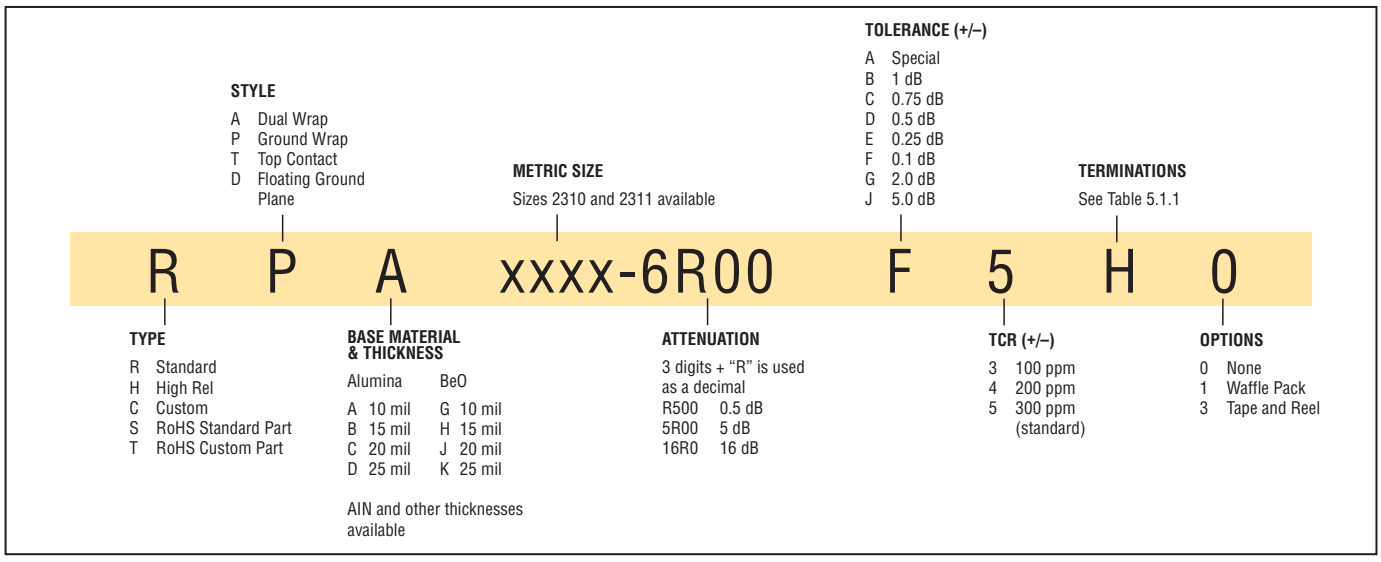


Figure 5.1.1: Part Numbering

LTCC Process

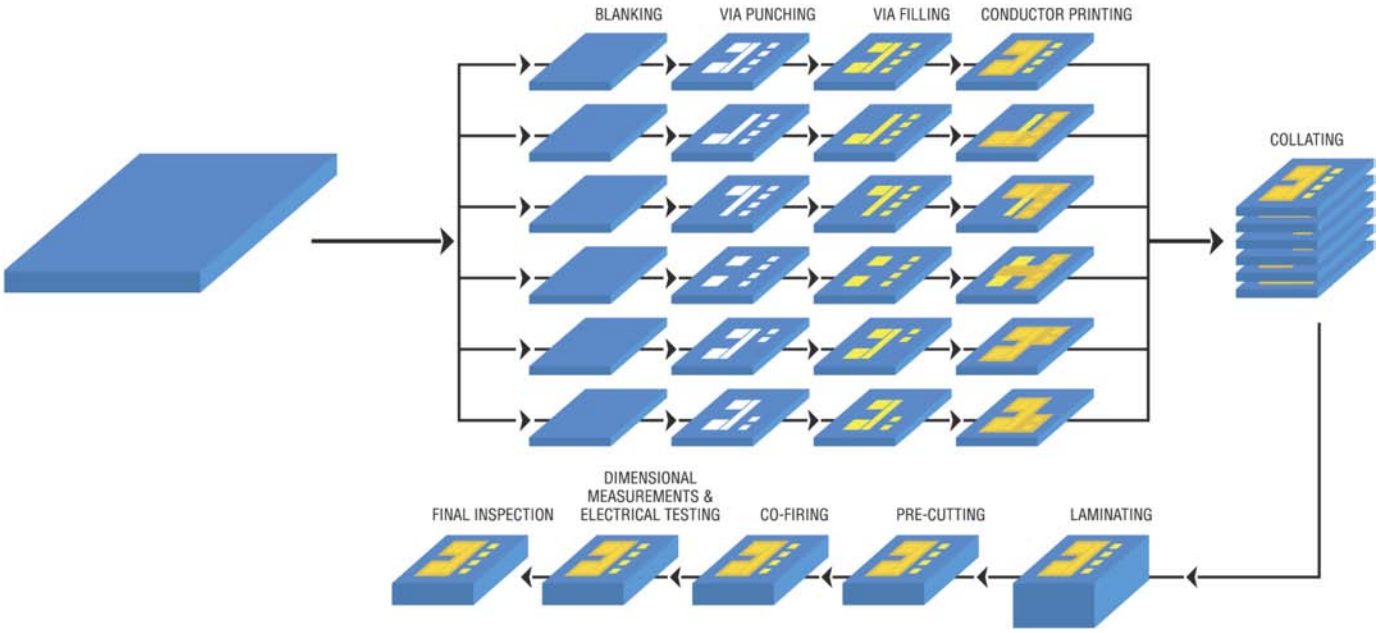


Figure 6.1.1: Typical Process for Fabricating an LTCC Structure
A series of steps are required for the production of LTCC structures. Performance, structure, and process capability of both ceramic and conductor are explained in the following pages.

Material Properties

Table: 7.1.1: Available Material Systems

Available Tape Systems	Available Metallization Systems
DuPont 951	All gold, all silver, ENiG
Ferro A6M	All gold

Table: 7.2.1: Material System Mechanical Properties

Parameter	DuPont 951	Ferro A6M
Green sheet area (inches^2)	6.5 & 8.0	6.5
Usable green sheet area (inches)	4.6 & 6.2	4.5
XY shrinkage	12.92%	14.85%
XY shrinkage tolerance	±0.3%	±0.3%
Green tape thickness (mils)	2, 4.5, 6.5, 10	5, 10
Fired tape thickness (mils)	1.7, 3.8, 5.5, 8.5	3.7, 7.4
Z shrinkage	15%	25%
Z shrinkage tolerance	±0.5%	±0.5%
Patterning technology	Screen Print & Etch	Screen Print
Thermal Conductivity	3.3	2.0
Young's Modulus (GPa)	120	92
Poisson's Ratio	—	—
Flexural Strength (MPa)	320	170
Density (g/cm^3)	3.1	2.5

Note:
1. 951 mechanical data taken from DuPont website

Table: 7.3.1: Material System Electrical Properties

Parameter	DuPont 951	Ferro A6M
Dielectric Constant @3GHz	7.8	5.6
Dielectric Constant tolerance	±0.2	—
Loss Tangent @3GHz	0.006	0.002
Breakdown voltage (V/25µm)	> 1000	> 900

Note:
1. Typical values are shown in this table.

Table: 7.4.1: Materials Options Preferred Material System

Manufacturer	DuPont	Ferro
Process	**951**	**A6M**
Inner Layer Au	TC502	30-025
Via Fill Au	TC501	30-078
Wirebond Co-Fire Au	5742 (Al wire) 5734 (Au wire)	30-065 (Al wire) 30-025 (Au wire)
Wirebond Post-Fire Au	5743 (Al wire) 5715 (Au wire)	30-068 (Al wire)
Solderable Au	5739 (Pt/Au)	36-020 (Pt/Au)
Brazing Material (AuSn, AuGe Braze)	5062/5063	4007
Inner Layer Ag	6142 (Signal) 6148 (Power, Gnd)	33-398
Via Fill Ag	6141 (Ag) 6138 (Pd/Ag)	33-343 (Ag) 39-005 (Pd/Ag)
Solderable Co-Fired Ag	6146 (Pd/Ag)	33-391
Solderable Post-Fired Ag	6135 (Pd/Ag)	3350
Co-Fired Resistors	CF Series	87 Series
Post-Fired Resistors	7200 Series	82 Series
Co-Fired Dielectric	9615	10-088
Post-Fired Overglaze	QQ550	NCA[a]

Note: a) NCA – Not currently available

Conductor Parameters

Anaren Ceramics characterizes the cross sectional shape of a conductor embedded in an LTCC substrate as an ellipse. Cross-sectional views of the conductors depict shapes that are not rectangular, but shapes with thicker mid-sections and tapered edges. Ellipses are traced around the conductor's outer edges and parameters such as width, thickness, and area is defined and based on the major and minor radii of the ellipses.

Conductor Line Widths and Spacings (minimums, typical, and tolerances)

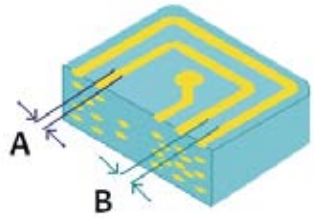


Figure 8.1.1: Line Width and Line to Line Spacing

Table 8.1.1: Line Width

	Minimum (mils)	Typical (mils)	Tolerance (mils)
(A)Printed	3.0	4.0	±1.0

Table 8.1.2: Line to Line Spacing

	Minimum (mils)	Typical (mils)	Tolerance (mils)
(B)Printed	3.0	4.5	±1.0

Notes:
1. Cross-sectional views of the conductors depict an elliptical shape – therefore conductor width is defined as the major diameter of a traced ellipse.
2. Printed parameters characterized in DuPont 951 all silver conductor system.
3. Printed parameters refer to a screen printing process.
4. Parameters are applicable to exposed and buried layers.

Conductor to Ceramic Edge (minimums, typical, and tolerances)

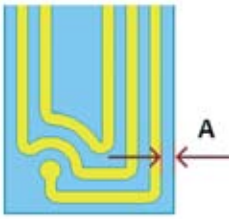


Figure 8.2.1: Conductor to Ceramic Edge

Table 8.2.1: Conductor to Ceramic Edge Parameters

	Minimum (mils)	Typical (mils)	Tolerance (mils)
(A)Printed	4.0	8.0	±1.0

Note:
Conductor thickness is defined as the minor radius of an ellipse at the center of the conductor.

Conductor Line Thickness and Shape (minimum, typical, and tolerances)

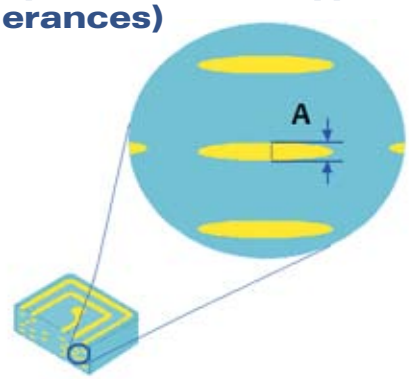


Figure 8.3.1: Conductor Thickness

Table 8.3.1: Conductor Thickness Parameters

	Minimum (mils)	Typical (mils)	Tolerance (mils)
(A)	0.4	0.5	±0.2

Note:
Conductor thickness is defined as the minor radius of an ellipse at the center of the conductor.

Conductor Cross-Sectional Area and Elliptical Dimensions (minimum, typical, and tolerances)

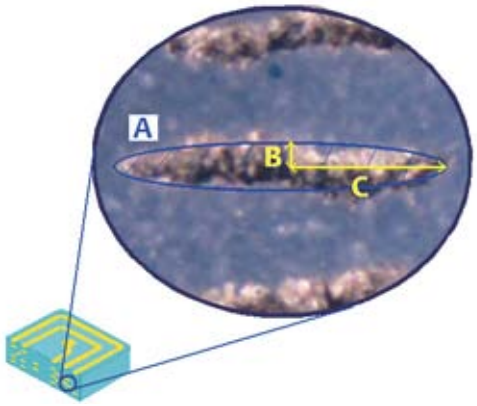


Figure 8.4.1: Cross-Section of a Conductor with a Traced Ellipse. The minor and major radius of the ellipse is shown. These radii define the thickness, width, and elliptical area of the conductor lines.

Table 8.4.1: Elliptical Parameters

	Minimum	Typical	Tolerance
(A) Elliptical Area (mils²)	0.9	1.80	—
(B) Minor Radius (mils)	0.2	0.25	±0.1
(C) Major Radius (mils)	1.5	2.25	±0.5

Notes:
1. Cross-sectional views of the conductors depict an elliptical shape – therefore the elliptical area served as an accurate measurement for its area.
2. The product of the major radius, minor radius, and π serve as the formula for calculating the elliptical area. $A = B.C.\pi$
3. The major and minor radius also serve as a mathematical model to define the cross-sectional shape of the conductors.

Conductor Layout Recommendations

The following are some general recommendations when laying out a multilayer circuit in LTCC.

1. Ground and power plane layout recommendations – keep metallization to <50% of ceramic area for better adhesion of ceramic layer to ceramic layer and for better consistency of shrinkage through a panel; for buried metal layers, see example in Figure 3.5.1. For best practices, use a hatched ground plane where possible.
2. Full metal coverage can be printed on exposed surfaces post firing.
3. Relative even distribution of metal on any tape layer is recommended for consistent ceramic shrinkage during firing.

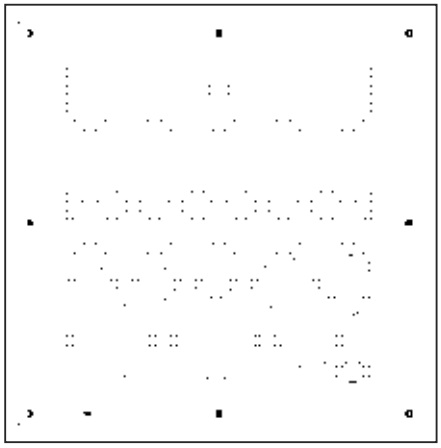


Figure 8.5.1: Buried Ground Plane, Metal Coverage <50%

> Shows solid ground plane in buried layer – % coverage in active area <50%.

> Metal is spread relatively evenly through the panel active area allowing even shrinkage.

Via Parameters

Via Diameter (minimums, typical, and tolerances)

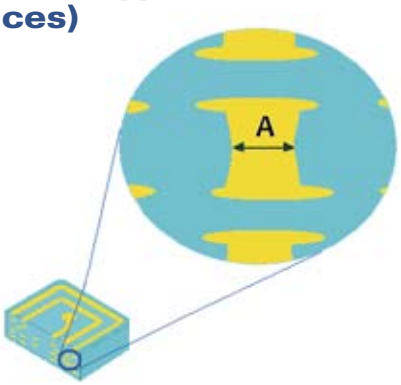


Figure 9.1.1: Diameter of Vias
Anaren defines via diameter as the narrowest point of the via transition form layer to layer. Typically there is a via capture pad on the interconnected layers. The via capture pad is larger in diameter than the via leading to the cross sectional pedestal shape shown.

Table 9.1.1: Via Diameter

	Minimum	Typical	Tolerance
(A) 2 mil Tape Thickness	3.4	4.5	±1
(A) 5 mil Tape Thickness	3.4	4.5	±1
(A) 10 mil Tape Thickness	6.8	8.5	±1

Notes:
1. Via diameter must be less than 80% tape thickness.

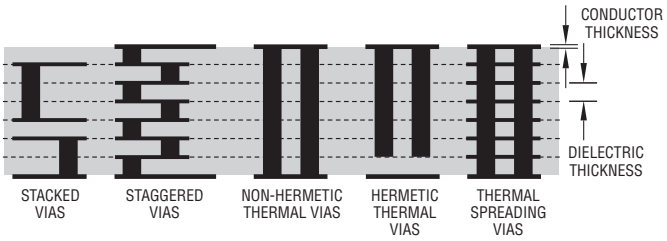


Figure 9.2.1: Vias Definition, Cross Section

Via Capture Pad (minimums, typical, and tolerances)

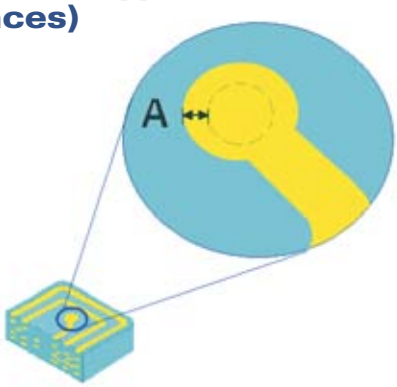


Figure 9.3.1: Via Capture Pad
Dashed line represents a via. Label (A) represents the distance from the via's edge to the edge of the capture pad.

Table 9.2.1: Via Capture Pads

Parameter	Minimum (mils)	Typical (mils)	Tolerance (mils)
(A) Via Capture Pad	2	3.5	±1.5

Notes:
1. No capture pad is needed unless a trace is connected to the via.
2. In some cases, capture pads are omitted by design – i.e. a trace that is less than the via diameter can run over the via as a means of connection.

Via Spacing and Layout (minimums, typical, and tolerances)

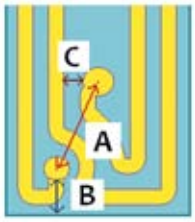


Figure 9.4.1: Via Spacing and Layout

Table 9.3.1: Via spacing and layout recommendations

Parameter	Minimum (mils)	Typical (mils)	Tolerance (mils)
(A) Via to Via Spacing	(1.5 x D) + D	—	±1
(B) Via to Conductor Edge	3	4	±1
(C) Via to Ceramic Edge	3	4	±1

Note:
1. Where "D" is via diameter.

Via Parameters *(continued)*

Table: 9.4.1: Design Guidelines Summary

Design Feature	Standard Guides	Premium Guides
Tape Layer Count	8-20 Layers	Up to 30 Layers[b]
Max. Substrate Size, Fired[a]	100 mm x 100 mm	100 mm x 100 mm
Thermal Vias, 95 μm Tape	250 μm Ø 10 mil	125 μm Ø 5 mil 250 μm pitch 10 mil
Thermal Vias, 215 μm Tape	250 μm Ø 10 mil	180 μm Ø 300 μm pitch
Distance, Conductor to Edge	250 μm min. 10 mil	175 μm min.
Internal Ground/ Power Plane Coverage	Grid: 50% Metal Localized: 100%	Grid: 50% Metal Localized: 100%
Minimum Tape Layer Count or Minimum Thickness	8 Layers or 1 mm, Whichever is More	8 Layers or 1 mm. Whichever is More

Notes: a) Typical with current tooling. Custom tooling will allow a maximum fired size of 160 x 160 mm. More complex size and shape designs can be addressed on an individual basis.
b) Up to 60 layers are possible with alternative processing techniques.

Cavities

> Cavities are defined as openings or through-holes in the LTCC design that are introduced into the green state structure prior to firing. Post-machined operations (CO_2 laser drilling) are not included in the recommendations below.

> Minimum distance of 100 mils must be maintained between adjacent cavities or through-holes, or between cavity walls or through-holes and the part.

> Minimum cavity length and width are 100 mils. Maximum ratio of cavity depth to minimum XY dimension is 1:1. Preferred ratio is 1:2. Minimum radius on any corner of a cavity is 20 mils.

> Cavities with floors must have a minimum floor thickness of 20 mils. Via and conductor limitations related to cavity walls or cavity shelves are the same as those listed in Table 9.4.1. Vias are listed in Table 8.2.1.

> Cavities may have one or more intermediate, stepped shelves. Minimum shelf thickness is 20 mils. Minimum shelf width is 50 mils.

> Maximum combined surface area of cavity opening to total part surface area is 60%. Preferred maximum is 40%.

Electroless Plating

> As a vertically integrated facility, Anaren Ceramics offers electroplating (Ni/Au and Ni/Pb-Sn), and electroless plating (Ni/Au).

Singulation

> Primary methods for component singulation are: laser machining and diamond saw, which may be used in combination.

> Singulation typically requires 60 mils of non-active area surrounding the final circuit. For complex shapes, CO_2 machining offers routing capability for the LTCC substrate.

> Products with wider mechanical tolerances can be green state singulation for cost reduction.

> Diamond saw dicing offers minimal dimensional deviation for standard, rectangular shapes.

Brazing

> Conductors for successful brazing to LTCC are available for the primary tape systems. Please refer to Table 2.4.1 for the specific material choices.

> To meet MIL Specification Visual Inspection Criteria, it is recommended that the brazing pad be 30-40 mils larger than the lead or seal ring component.

> Gold-tin or gold-germanium soldering is recommended for most applications. Anaren Ceramics has soldering capability for those customers requiring a completed package.

Testing

> DC electrical testing can be achieved with either an electrical Net test (opens and shorts) or capacitor test. It is required that the customer supply an ASCII Netlist per 356D.

Passive Elements

> Inductors, resistors, and capacitors may all be integrated into a standard LTCC structure. Electrical characteristics are achieved through a combination of design (e.g., surface real estate, one or more layers), inherent properties of the green tape, and the material system chosen.

> Depending upon the material system, enhancement materials exist to locally increase the dielectric constant for some capacitor ranges. Specifics must be reviewed on a design-by-design basis.

> Buried resistors will exhibit a tolerance of ±30%. Surface resistors may typically be laser trimmed using a Nd:YAG laser to ±2% to ±5%. Tighter tolerance requirements must be reviewed on a design-by-design basis. Resistor values are limited by design and material availability, but typically run between 10 Ω and 1 kΩ for buried resistors, and 1 Ω to 100 MΩ for surface resistors. Minimum buried resistor size is 30 x 30 mils; minimum surface resistor size is 20 x 20 mils.

> Overcoat and solder-blocking materials are available as post-fired operations.

Multilayer Parameters

Tape Layer Thickness (minimum, typical, and tolerances)

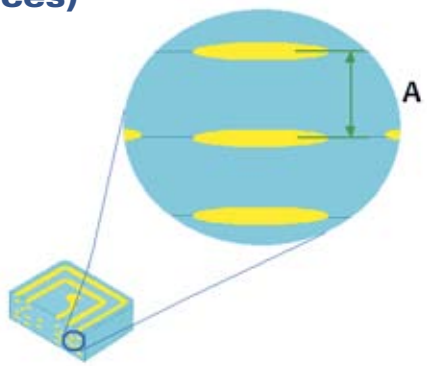


Figure 10.1.1: Ceramic Tape Layer Thickness

Table 10.1.1: Ceramic Tape Layer Thickness

Parameter	Minimum (mils)	Typical (mils)	Tolerance (mils)
(A) Tape thickness 2 mil	1.45	1.7	±0.25
(A) Tape thickness 4.5 mil	3.55	3.8	±0.25
(A) Tape thickness 10 mil	8.25	8.5	±0.25

Notes:
1. Tape thickness is defined as the distance between the centers of conductors in a successive layer.
2. Combinations of tape may be used to achieve alternative desired thickness.

Conductor and Tape Collation/ Layer to Layer Alignment (tolerance)

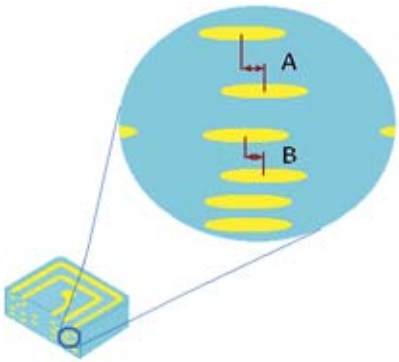


Figure 10.2.1: Layer to Layer Alignment

Table 10.2.1: Layer to Layer Alignment

Parameter	Tolerance (mils)
(A & B) Layer to layer alignment	±2.0

Dielectric Constant Measurements

Ring Resonators are used to measure the dielectric constant of available material sets. A ring resonator is a simple structure that is a 50Ω transmission line, one wavelength long at a fundamental frequency. The single wavelength transmission line ring has no discontinuity effects resulting in a standing wave pattern that resonates at every harmonic of the fundamental frequency. There is no reflection characteristic on the ring structure resulting in full wavelength resonances only. Energy is coupled onto and off the ring through two identical transmission lines that are seperated from the ring by a 4 mil gap, resulting in a capacitive coupling effect. The dielectric constant information is extracted from the frequency of resonance at each harmonic allowing multiple D_K (dielectric constant) estimates per structure. This information is somewhat independent of the quality of the transmission line print allowing a very accurate estimate of the material D_K.

Microstrip and Stripline ring resonators have been designed, fabricated and measured yielding D_K data for DuPont 951 material sets. D_K is extracted from resonant frequency measurements using the following equations:

Table 11.1.1: D_K and effective D_K:

STRIPLINE RING RESONATORS
Material $D_K = (c*n/(f_c*l))^2$
MICROSTRIP RING RESONATORS
Effective $D_K = (c*n/(f_c*l))^2$
PARAMETERS
$c = 3.0*10^8$ (m/s)
n = Harmonic number
f_c = Measured harmonic resonant frequency (Hz)
l = Resonator length (m)

Dual ring resonator coupons designed to resonate at fundamental frequencies of 2, 3, 5, 7 and 11 GHz have been manufactured and RF tested at Anaren Ceramics. The resonator coupon contains a microstrip structure and a stripline structure, forming two ring resonators in one block of ceramic. Figure 6.1.1 shows a single dual resonator coupon; figure 6.1.2 shows a cross section of the dual resonator structure. Figure 6.1.3 shows a typical broadband 5GHz ring resonator response.

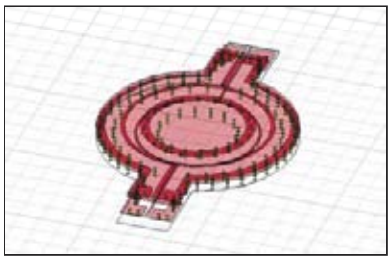


Figure 11.1.1: Dual Ring Resonator Structure

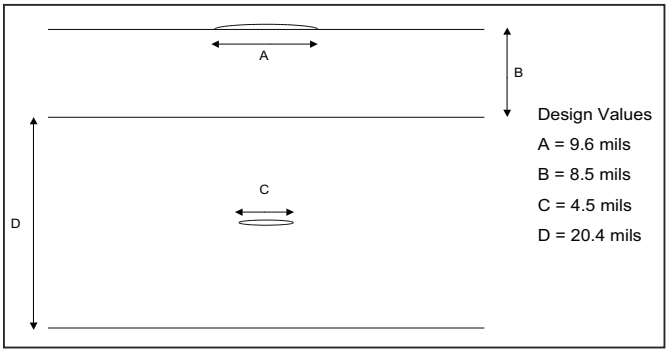


Figure 11.1.2: Transmission Line Dimensions – DuPont 951.

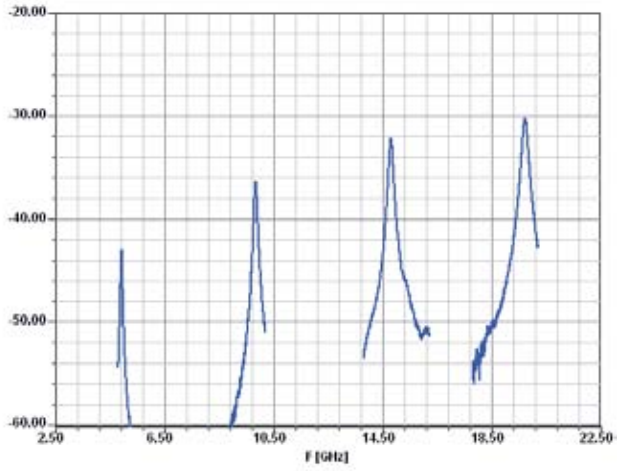


Figure 11.1.3: Typical Broadband 5GHz Ring Resonator Response showing resonances at the first/second/third and fourth harmonics.

The ring resonator coupons can be used to estimate lot to lot material dielectric constant (D_K) and effective D_K at multiple frequencies; the 5GHz resonator has recently been used as a means of comparing process variation between firing processes in a box oven and on a belt furnace.

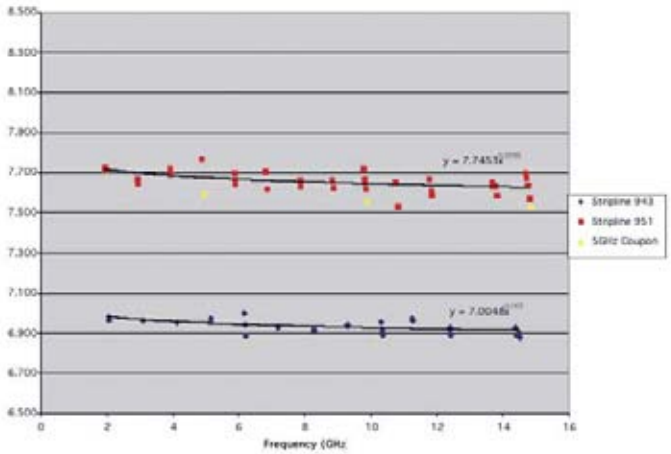


Figure 11.1.4: D_K Estimates for DuPont 943 and DuPont 951 from stripline ring resonator measurements

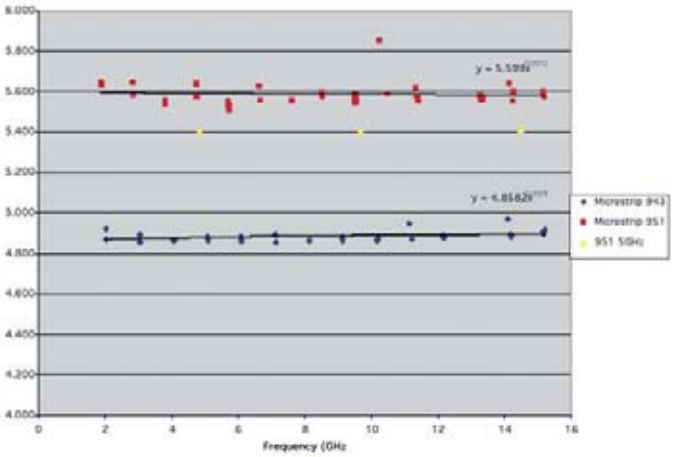


Figure 11.1.5: Effective D_K Estimates for DuPont 943 and DuPont 951 from microstrip

Attenuation Per Unit Length vs. Frequency Measurements

Attenuation Lines: 50Ω Microstrip and Stripline transmission lines are used to measure attenuation vs. frequency. Lines of varying lengths are measured up to 20GHz and compared to each other. All attenuation line data is normalized to a unit length of one inch.

Table 11.2.1: Attenuation line lengths

	Microstrip Line Length (inches)	Stripline Line Length (inches)
Line 1	1.0	1.1
Line 2	1.0	1.1
Line 3	1.76	1.86
Line 4	1.76	1.86
Line 5	3.79	3.89
Line 6	16.35	16.45
Line 7	9.63	9.73

Table 11.2.2: Calculated attenuation/unit length for DuPont 951 stripline and microstrip transmission lines

Frequency (GHz)	Microstrip Attenuation/unit length (dB)	Stripline Attenuation/unit length (dB)
2	-0.15	-0.24
3	-0.19	-0.29
4	-0.23	-0.35
5	-0.28	-0.40
6	-0.32	-0.46
7	-0.36	-0.52
8	-0.40	-0.57
9	-0.45	-0.63
10	-0.49	-0.68
11	-0.53	-0.74
12	-0.57	-0.80
13	-0.62	-0.85
14	-0.66	-0.91
15	-0.70	-0.96

Attenuation per unit length is an average of six line measurements – lines having differing lengths. Microstrip transmission lines are ~9mils in width and 0.5mils in thickness; stripline transmission lines are ~4.5mils in line width and 0.5mils in thickness.

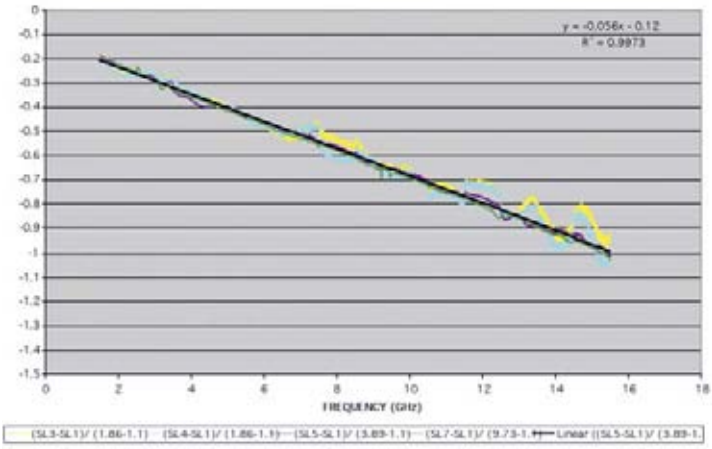


Figure 11.2.1: DuPont 951 Stripline Attenuation Lines – attenuation per unit length

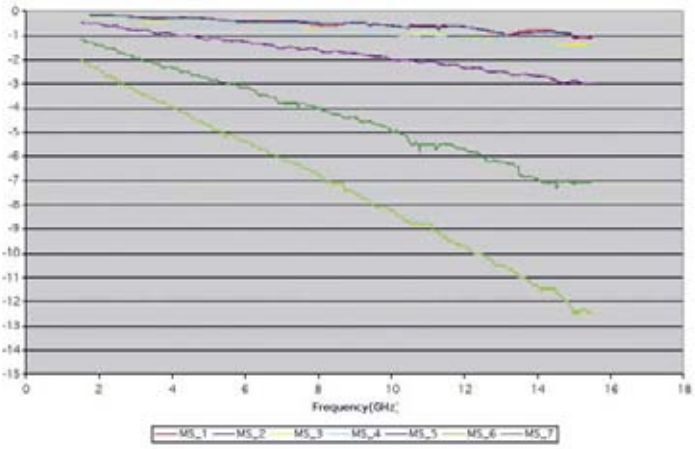


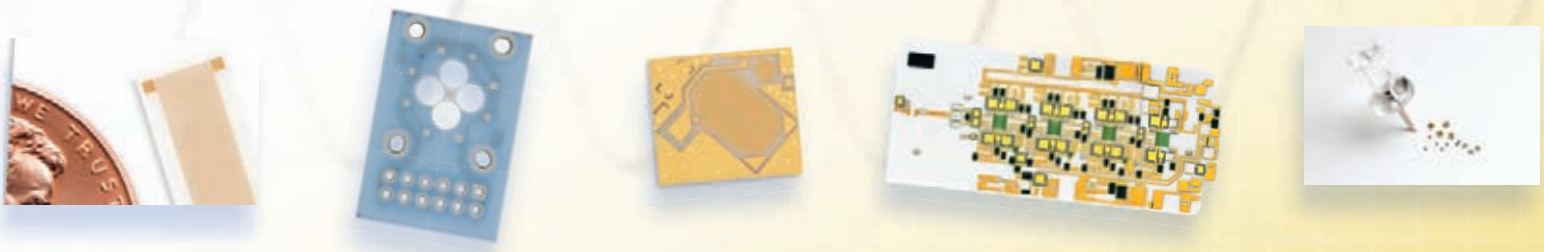
Figure 11.2.2: DuPont 951 Microstrip Attenuation Lines – attenuation per unit length

Best Practices

1. In areas where there is a crossover, active conductor traces should be coated with solder mask.
2. Components less than .080" x .050" attached with conductive epoxy should have a solder mask between the attached pads.
3. For multilayer structures, we recommend a 2 mil pullback of dielectric layer for each consecutive dielectric print.
4. When creating a crossover dielectric, it is a good idea to put a barrier in between the 2 crossovers to prevent shorts between adjacent traces (see page 5).
5. Don't put silver material beneath gold conductors separated by dielectric, to avoid Kirkendall voiding.
6. Do not design resistors in close proximity to a multilayer structure such as a printed capacitor.
7. If possible, use similar layer-to-layer count on both sides of a substrate to minimize potential for bowing of substrate.
8. For cost reduction, keep resistors in same orientation on circuit board.
9. For cost reduction and maximum resistor value consistency, alter the aspect ratio to achieve different resistor values with the same paste.

Notes

Cost competitive



Deep RF & microwave expertise

Anaren Ceramics highlights!

- > Multilayer, double-sided thick film substrates
- > Photo Imageable dielectrics for reduced via size and spacing in multilayers
- > Lower-cost microwave circuitry, featuring advanced etching technology (APECS)
- > LTCC substrates up to 30 layers
- > Etched line width and spacing — controlled to an order of magnitude better than traditional screen printing for lower-loss, higher-density circuits
- > Alumina substrates 96%, 99.5%, and 99.6%
- > Ferrite, Beryllia Oxide, Aluminum-nitride substrates
- > Lines and spaces down to 0.8 mils
- > Edge wraps and metallized substrate vias
- > In-house plating: gold-tin, matte-tin, tin-lead, electroless nickel-gold
- > Specific metallizations for wire bonding, soldering, or brazing
- > Integrated laser-trimmed resistors
- > Integrated laser marking and serialization
- > Integrated capacitors, inductors, and thermistors
- > Machining of substrates to any shape
- > Proprietary method for creating structures with blind features such as open cavities and counterbores
- > Net testing
- > RoHS/Reach compliant material sets available
- > ISO-9001:2008 registered facility
- > Vertical integration: All processes from CAD to shipped product are performed in-house
- > Microwave modeling, design and test capability
- > Circuit layout assistance
- > Extensive industry experience in materials, ceramics, and microelectronics design
- > Standard and custom chip resistors and attenuators, plus QPL-listed chips per DESC MIL-PRF-55342

We're ready to help!
Whatever you're thinking, we're ready with information, design assistance, samples, quotations — anything and everything you need to develop those never-before-possible solutions.

Simply call us at 603-898-2883, e-mail us at ceramics@anaren.com, or visit www.anaren.com/Ceramics.

Proven & reliable

Anaren®
What'll we think of next?®

800-411-6596 > www.anaren.com

Anaren Ceramics, Inc.
27 Northwestern Drive
Salem, NH 03079
Tel: 603-898-2883
Fax: 603-898-4273
Email: ceramics@anaren.com

Anaren, Inc.
6635 Kirkville Road
East Syracuse, NY 13057
Tel: 315-432-8909
Toll free: 800-411-6596
Email: sales@anaren.com